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HIGH DENSITY

CIRCUIT TECHNOLOGY

PART IV

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16. ABSTRACT

The objectives of this part of the contract effort was to conduct an accurate study and evaluation of dielectric thin films in order to find the material or combination of materials which would optimize NASA's double layer metal process. Emphasis was placed on polyimide dielectrics because of their reported outstanding dielectric characteristics (including electrical, chemical, thermal, and mechanical) and ease of processing, as well as their rapid acceptance by the semiconductor industry.

The following dielectric materials were evaluated:

a. Atmospheric CVD silicon dioxide (phosphorous doped)
b. Polyimides (Hitachi PIQ-13 and Dupont PI-2545 and PI-2555)
c. Low pressure CVD silicon dioxide (both doped and undoped varieties)
d. Sputtered quartz (undoped)
e. Plasma deposited silicon dioxide (both doped and undoped from two different vendors)
f. Plasma deposited silicon nitride
g. Polyimides and composites of polyimides with all of above.

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FORWARD

This report describes a portion of the work performed from July 1980 to March 1982 under Contract NAS8-33448 for the George C. Marshall Space Flight Center, National Aeronautics and Space Administration, Marshall Space Flight Center, Alabama. The technical managers for MSFC were Mr. B. R. Hollis, Jr., Mr. R. F. Dehaye and Mr. J. M. Gould. This report was prepared by the Microelectronics Research Laboratory of the Department of Electrical Engineering, Mississippi State University, under the direction of the principal investigator Dr. Thomas E. Wade. The principal participants in the program were Mrs. Mildred N. Sellars and Mr. James Ebentier.

This final report has been divided into four areas of emphasis, with a separate comprehensive report for each area. These four areas represent the following subject groupings:

PART I. Emphasis is on the realization of very dense metal interconnection for VLSI systems utilizing the lift-off process. Both a survey of lift-off techniques is presented as well as experimental and novel lift-off methods which have been investigated by the author.

PART II. Emphasis here is on multilevel metal interconnection system for VLSI systems utilizing polyimide as the interlayer dielectric material. A complete

characterization of polyimide materials is presented as well as experimental methods accomplished using a double level metal test pattern. A novel double exposure polyimide patterning process is also presented.

PART III. Emphasis is on dry plasma processing including a characterization of and an equipment survey for plasma etching, reactive ion etching, (reactive) ion milling and plasma deposition processes. Also included is an indication of future microelectronic trends, including patterning technology, lithography, materials deposition, packaging, etc.

PART IV. Emphasis here is on an evalution of dielectric material for use in VLSI metal interconnection systems. A number of dielectric material types (or combination of materials) are experimentally evaluated using a second test pattern. Recommendations are presented based on these findings.

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I. INTRODUCTION

The objectives of this part of the contract effort was to conduct an accurate study and evaluation of dielectric thin films in order to find the material or combination of materials which would optimize NASA's double layer metal process. Emphasis was placed on polyimide dielectrics because of their reported outstanding dielectric characteristics (including electrical, chemical, thermal, and mechanical) and ease of processing, as well as their rapid acceptance by the semiconductor industry.

The following dielectric materials were evaluated:

a. Atmospheric CVD silicon dioxide (phosphorous doped)

b. Polyimides (Hitachi PIQ-13 and Dupont PI-2555 and PI-2545)

c. Low pressure CVD silicon dioxide (both doped and undoped varieties)

d. Sputtered quartz (undoped)

e. Plasma deposited silicon dioxide (both doped and undoped from two different vendors)

f. Plasma deposited silicon nitride

g. Composite films of polyimide and atmospheric CVD silicon dioxide

Composite films of polyimide and LPCVD silicon dioxide (doped/undoped)

Composite films of polyimide and sputtered quartz

Composite films of polyimide and plasma deposited silicon dioxide

Composite films of polyimide and plasma deposited silicon nitride

h. All of above films over thin aluminum for pin-hole evaluation.

Over 200 wafers have been prepared utilizing these dielectric materials such that a thorough characterization and evaluation may be conducted. Based upon these findings, certain dielectrics are recommended for NASA's use in their custom VLSI MOS arrays which will be yield efficient, reliable (short and long term life tested), and hence economical.

II. EXPERIMENTAL PROCEDURE

A. General Setup

In this experimental study, 10 lots of 25 each 3 inch Monsanto silicon wafers having a resistivity of 9-15 ohm-cm., orientation <111> and boron doping were used as substrate material. These ten lots were designated as MS1 through MS10. Two lots, MS6 and MS10 were used for process development of the polyimide materials and test wafers. Lot MS4 was used for pinhole density determination test and dielectric adhesion studies. All wafers used in this study were furnished by Applied Micro Circuits Corporation of San Diego, California.

All wafers were thermally oxidized at the outset using a Thermco furnace set at 1050°C and a 15 minute dry O_2, 120 minute steam, 15 dry O_2 and a 20 minute N_2 anneal process resulting in approximately 7500Å thick oxide. Oxide and other dielectric measurements were made with a Nanometrics Nano Spec/AFT Micro Area Gauge and a Nanometrics CTS-102 Film Thickness instrument. The pinhole decoration wafers, Lot MS4, were thermally oxidized with only 1200 Å of oxide (royal blue color in white light) and a subsequent 2000 Å Al/Si metal DC sputtered on them.

Metallization of all wafers was accomplished in an MRC 603 vertical sputter system at approximately 8 kilowatt deposition power and 12 millitorr pressure. Patterning of aluminum (and dielectric) thin films was accomplished with positive photoresist and a Perkin-Elmer 140 microalign projection exposure system.

Most dielectrics used in this study were deposited at different semiconductor related vendors—as indicated in Wafer Process List, section C—using the vendors demonstration equipment. Atmospheric CVD phosphorous doped oxides deposited using an AMS 2000 Reactor at 450°C and all polyimides (Hitachi PIQ and Dupont PI 2545 and PI 2555) were processed at Applied Micro Circuits Corporation. Low pressure CVD oxides were deposited using an Applied Crystal Science SPLTO Reactor (diffusion tube type) at 420°C, 320 millitorr and 4% by mol. weight phosphorous doped. Plasma enhanced nitrides were deposited by the LFE Corporation using their System 8000 reactor at 340°C, and 600 watts. The plasma enhanced oxides were deposited primarily

by Pacific Western Systems, Inc. in their Coyote Reactor at 380°C and a pressure of approximately 1 torr. A few plasma deposited oxide wafers were processed at LFE Corp. at 340°C, 45 watts power level. The sputtered quartz was deposited at Varian Corp. using their model 3125 RF S-Gun System with revolving planetary system. Wafers are heated to approximately 150-200°C during deposition and result in an oxide composite of SiO_x where $X \simeq 1.3$. For all composite materials (i.e., deposition of 4000 Å atmospheric CVD oxide followed by a 1 μ thick layer of Dupont PI 2555 polyimide), the first layer was deposited and via holes (and pads) were patterned prior to depositing and patterning the second dielectric material.

Both first (1 μ thick) and second (1.5 μ thick) level metal layers consist of aluminum with 1% silicon. In order to obtain low ohmic resistance between these two levels in via's (opening in the dielectric to allow first and second level continuity), a RF sputter etch step is incorporated in-situ prior to depositing the second level metal. In processing some of the wafers for this study, the sputter etch step was inadvertantly left out. This resulted in via chains having very high resistance (open-circuited) which could not be broken down by either increased anneal temperature and time or by applying a d.c. bias.

B. Test Mask Description

The test mask used in evaluating these dielectrics consisted of several areas as follows:

AREA I. Via Test Pattern. Consist of a chain of 400, 600, 1000 2000 via's all 8 x 8 microns square. Also, small chain of 10 via's both 8 x 8 and 6 x 6 microns in size.

AREA II. Capacitor Short Check. Consist of first and second level metal capacitor plates of area 1194 $mils^2$ or 770,625 microns square. Second metal overlaps first metal by 10 microns all around.

AREA III. Cross-Over Test Area. Consist of 8442 cross-overs having first level metal 5 microns wide and 139,700 microns long, and second level metal 8 microns wide and 84,350 microns long. Total cross-over area is 337,680 square microns (523.3 square mils).

AREA IV. Interdigitated Metal. For each level of metal, unconnected interdigitated metal patterns are formed, each half of the pattern being connected to a pad. First level metal pattern consist of 19,000 micron (748 mils) long, 5 micron wide with 5 micron spaces. Second level metal pattern consist of 12,160 micron (479 mils) long, 8 microns wide with 8 micron spaces.

AREA V. Metal Resistivity Monitoring Pattern. For each level of metal, a pattern consisting of three pads is used to monitor the resistivity of that levels metal. Between the first two pads, 35 squares of metal exist. Between the first and third pad, 74 squares of metal exist. By

measuring the resistance between these two sets of pads, the metal ohms per square may be determined excluding contact resistance of the measuring probes. The width of these first and second level metal runs is 50 microns.

C. Wafer Process List

The following wafers have been processed for accurate comparison of the most promising dielectrics based on extensive literature searches:

1. Atmospheric Chemical Vapor Deposited Silicon Dioxide, Atm. SiO_2

Source: Applied Micro Circuits Corporation
8808 Balboa Avenue
San Diego, CA 92123

17 wafers, 1μ thick phosphorous doped (MS1-1 thru 17)

6 wafers, 0.4μ thick phosphorous doped for PI composit
2-PIQ 13 wafers 9-1, 9-2
2-PI 2555 wafers 9-3, 9-4
2-PI 2545 wafers 9-5, 9-6

6 wafers, 0.4μ thick phosphorous doped over PI
2-PIQ 13 wafers 9-7, 9-8
2-PI 2555 wafers 9-9, 9-10
2-PI 2545 wafers 9-11, 9-12

1 wafer for pinhole density determination

1 wafer, 0.4μ thick vapox then PIQ 13, 4-20

2. Low Pressure Chemical Vapor Deposited Silicon Dioxide LPCVD-SiO_2

Source: Applied Crystal Science
2035 O'Toole Avenue
San Jose, CA 95131
ATTN: Chris Guiver (408)946-9353

6 wafers, 1μ thick phosphorous doped (3-4% mol. wt.)
(wafers 2-8, 2-9, 2-10, 2-11, 2-12, 2-14)

6 wafers, 1μ thick undoped (wafers 2-7, 2-16, 2-17, 2-21, 2-22, 2-23)

6 wafers, 0.25μ thick phosphorous doped (for PI composit)
2-PIQ 13 wafers 2-13, 2-15
2-PI 2555 wafers 2-18, 2-19
2-PI 2545 wafers 2-20, 2-24

6 wafers, 0.25μ thick undoped (for PI composit)
2-PIQ 13 wafers 2-1, 2-2
2-PI 2555 wafers 2-3, 2-4
2-PI 2545 wafers 2-5, 2-6

6 wafers, 0.25μ thick phosphorous doped over PI
2-PIQ 13, wafers 7-1, 7-2
2-PI 2555, wafers 7-5, 7-7
2-PI 2545, wafers 7-9, 7-10

6 wafers, 0.25μ thick undoped over PI
2-PIQ 13, wafers 7-13, 7-3
2-PI 2555, wafers 7-6, 7-17
2-PI 2545, wafers 8-6, 8-7

4 wafers for pinhole density determination
2 wafers with 1μ phosphorous doped LPCVD SiO_2 (4-6, 4-7)
1 wafer with 0.25μ phosphorous doped for PI composit (4-8)
1 wafer with PIQ 13 then 0.25μ phosphorous doped (4-16)

3. Plasma Enhanced Silicon Dioxide, P.E. SiO_2

Source: Pacific Western Systems, Inc.
505 East Evelyn Avenue
Mountain View, CA 94041
ATTN: John Ronald (415) 961-8855

6 wafers, 1μ thick phosphorous doped (3-4% mol. Wt.)
(wafers 3-3, 3-12, 3-19, 3-20, 3-21, 3-23)

6 wafers, 1μ thick undoped
(wafers 3-11, 3-9, 3-14, 3-17, 3-22, 3-24)

6 wafers, 0.25 thick phosphorous doped (for PI composit)
2-PIQ 13, wafers 3-1, 3-6
2-PI 2555, wafers 3-8, 3-10
2-PI 2545, wafers 3-15, 3-18

6 wafers, 0.25 μ thick undoped (for PI composit)
2-PIQ 13, wafers 3-2, 3-4
2-PI 2555, wafers 3-5, 3-7
2-PI 2545, wafers 3-13, 3-16

6 wafers, 0.25μ thick phosphorous doped over PI
2-PIQ 13, wafers 7-15, 7-16
2-PI 2555, wafers 7-8, 7-18
2-PI 2545, wafers 7-11, 7-12

5 wafers, 0.25μ thick undoped over PI
2-PIQ 13, wafers 7-4, 7-14
2-PI 2555, wafers 8-11, 8-12
1-PI 2545, wafers 7-24

4 wafers for pinhole density determination
2 wafers with 1μ phosphorous doped P.E. SiO_2 (4-9, 4-10)
1 wafer with 0.25μ phosphorous doped for PI composit (4-11)
1 wafer with PIQ 13 then 0.25μ phosphorous doped (4-17)

Also sent 3 wafers to Bill Liggett, LFE, for plasma enhanced SiO_2 deposition as follows:

2 wafer, 1μ thick undoped, wafer 3-25, 5-25
1 wafer, 0.25μ thick undoped (for PI composit), wafer 7-25

4. Sputtered Quartz SiO_x

Source: Varian Corporation
611 Hansen Way
Palo Alto, CA 94303
ATTN: Dennis Nichols
(415) 493-4000 Ext. 3826

7 wafers, 5000 Å thick (MS 5-13 thru 19)

5 wafers, 1000 Å thick for PI composit
2-PIQ 13 wafers 5-20, 5-21
2-PI 2555 wafers 5-22, 5-23
1-PI 2545 wafers 5-24

6 wafers, PI then 1000 Å thick quartz
2-PIQ 13 wafers 8-2, 8-3
2-PI 2555 wafers 8-4, 8-5
2-PI 2545 wafers 8-14, 8-15

3 wafers for pinhole density determination
1 wafer with 5000 Å quartz, wafer 4-14
1 wafer with PIQ 13 then 1000 Å quartz, 4-19
1 wafer with 1000 Å quartz for PI composit, 4-15

5. Plasma Enhanced Silicon Nitride, P.E. Si_xN_y

Source: LFE Corporation
3375 Scott Blvd.
Suite 102
Santa Clara, CA 95051
Attn: William T. Liggett
(408) 727-2360

6 wafers, 1μ thick P.E. Si_xN_y (MS 5-1 through 6)

6 wafers, 0.25μ thick for P.I. composit
3-PIQ 13 wafers 5-8, 5-11, 5-12
2-PI 2555 wafers 5-9, 5-10
1- PI 2545 wafer 5-7

6 wafers, P.I. then 0.25μ thick P.E. Si_xN_y
2-PIQ 13 wafers 8-8, 8-10
2-PI 2555 wafers 7-19, 7-20
2-PI 2545 wafers 7-21, 7-22

3 wafers for pinhole density determination
1 wafer with 1μ PE Si_xN_y (4-12)
1 wafer with 0.25μ for P.I. composit (4-13)
1 wafer with PIQ 13 then 0.25μ P.E. Si_xN_y (4-18)

6. Polyimides, Hitachi PIQ-13 and Dupont PI 2545 and PI 2555

Source: Applied Micro Circuits Corporation
and
Mississippi State University

2 wafers, 0.5μ thick PIQ 13 (9-13, 9-14)

2 wafers, 0.5μ thick PI 2555 (9-15, 9-16)

2 wafers, 0.5μ thick PI 2545 (9-17, 9-18)

2 wafers, 0.75μ thick PIQ 13 (9-19, 9-20)

2 wafers, 0.75μ thick PI 2555 (9-21, 9-22)

2 wafers, 0.75μ thick PI 2545 (9-23, 9-24)

2 wafers, 1.0μ thick PIQ 13 (9-25, 8-16)

2 wafers, 1.0μ thick PI 2555 (8-17, 8-18)

2 wafers, 1.0μ thick PI 2545 (8-19, 8-20)

2 wafers, 1.25μ thick PIQ 13 (8-21, 8-22)

2 wafers, 1.25μ thick PI 2555 (8-23, 8-24)

2 wafers, 1.25μ thick PI 2545 (8-25, 2-25)

4 wafers for pinhole density determination
- 1 wafer with 0.75μ thick PIQ 13 (4-21)
- 1 wafer with 1.25μ thick PIQ 13 (4-23)
- 1 wafer with 0.75μ thick PI 2555 (4-22)
- 1 wafer with 1.25μ thick PI 2555 (4-24)

2 wafers, 2.0μ thick PIQ 13 (8-1, 8-13)

2 wafers, 2.0μ thick PI 2555 (10-4, 10-6)

2 wafers, 2.0μ thick PI 2545 (10-8, 10-23)

D. Restricted Wafer List Studied

Of the some 200 wafers processed, over 200 die per wafer were realized. In collecting data for the dielectric comparative studies, over 40 measurements per die is required (resistance, leakage currents and breakdown voltage measurements for capacitor, cross-over, interdigitated fingers, via chain as well as capacitance of big capacitor for five different anneal temperatures) resulting in over 1.5 million measurements. Since collecting and analyzing this amount of data within the time frame required was impossible, the number of wafers studied was decreased to 30 representative dielectrics, in addition to those in lot M4 which were used for pin-hole and dielectric adhesion studies. For ease of reference, the dielectrics have been coded as indicated in Table 1, and the actual wafers studied are listed in Table 2.

TABLE I - WAFER CODE

Wafer Type	Code
Doped Atmospheric CVD SiO_2	D-Ox
Doped LPCVD SiO_2	D-LP-Ox
Undoped LPCVD SiO_2	U-LP-Ox
Doped Plasma Enhanced SiO_2	D-PE-Ox
Undoped Plasma Enhanced SiO_2	U-PE-Ox
Sputtered Quartz	Qtz
Plasma Enhanced Si_xN_y	PE-Nit
Hitachi PIQ-13	PIQ
Dupont PI-2545	2545
Dupont PI-2555	2555

TABLE 2 - WAFER TYPE

Wafer No.	Type
1-7	1μ D-Ox
9-2	0.4μ D-Ox + 0.7μ PIQ
9-8	0.9μ PIQ + 0.5μ D-Ox
2-22	1μ U-LP-Ox
2-8	1μ D-LP-Ox
2-15	0.25μ D-LP-Ox + 1μ PIQ
2-2	0.25μ U-LP-Ox + 1μ PIQ
7-2	0.7μ PIQ + 0.25μ D-LP-Ox
7-13	0.6μ PIQ + 0.25μ U-LP-Ox
3-23	0.95μ D-PE-Ox
3-9	1.1μ U-PE-Ox
3-6	0.25μ D-PE-Ox + 0.9μ PIQ
7-25	0.25μ U-PE-Ox + 0.9μ PIQ

TABLE 2 - WAFER TYPE (Continued)

Wafer No.	Type
7-15	0.6μ PIQ + 0.25μ D-PE-Ox
7-14	0.6μ PIQ + 0.25μ U-PE-Ox
3-25	0.8μ U-PE-Ox
5-14	0.35μ Qtz
5-21	0.1μ Qtz + 0.9μ PIQ
8-3	0.6μ PIQ + 0.1μ Qtz
5-3	1.0μ PE-Nit
5-12	0.25μ PE-Nit + 0.9μ PIQ
8-10	0.6μ PIQ + 0.2μ PE-Nit
9-16	1.0μ 2555
9-25	0.8μ PIQ
8-18	1.5μ 2555
8-20	1.1μ 2545
8-22	1.2μ PIQ
8-24	1.5μ 2555
8-25	1.25μ 2545
8-13	1.7μ PIQ

E. Test Setup

The test setup for monitoring breakdown voltages, leakage currents and via chain resistances is shown pictorially in Figures 1 through 3. An Electroglas probe station was used in conjunction with a Keithley 416 Electrometer (for current leakage measurements) and other precision voltage, capacitance and resistance measurement apparatus.

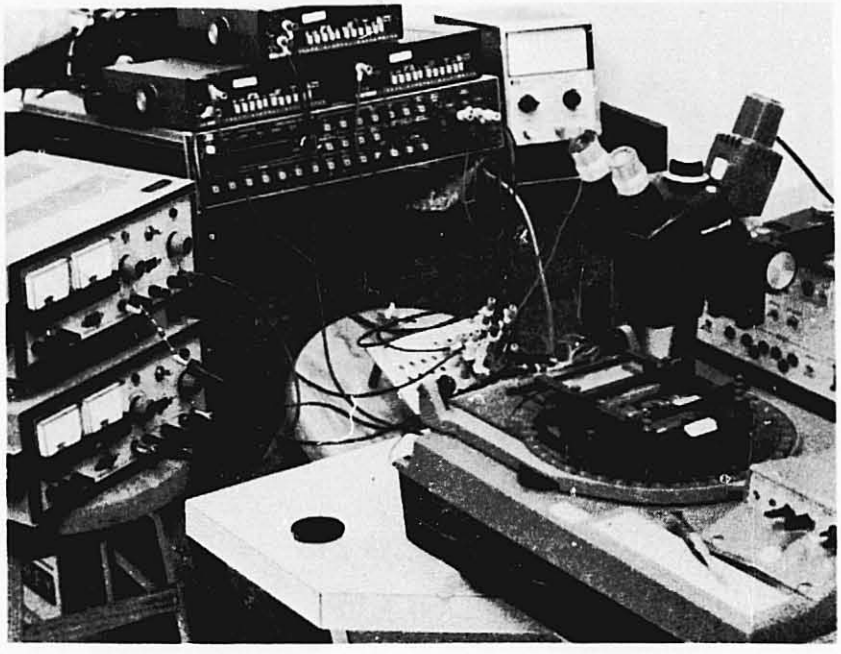


Figure 1. Test set-up for making break-down voltage measurements.

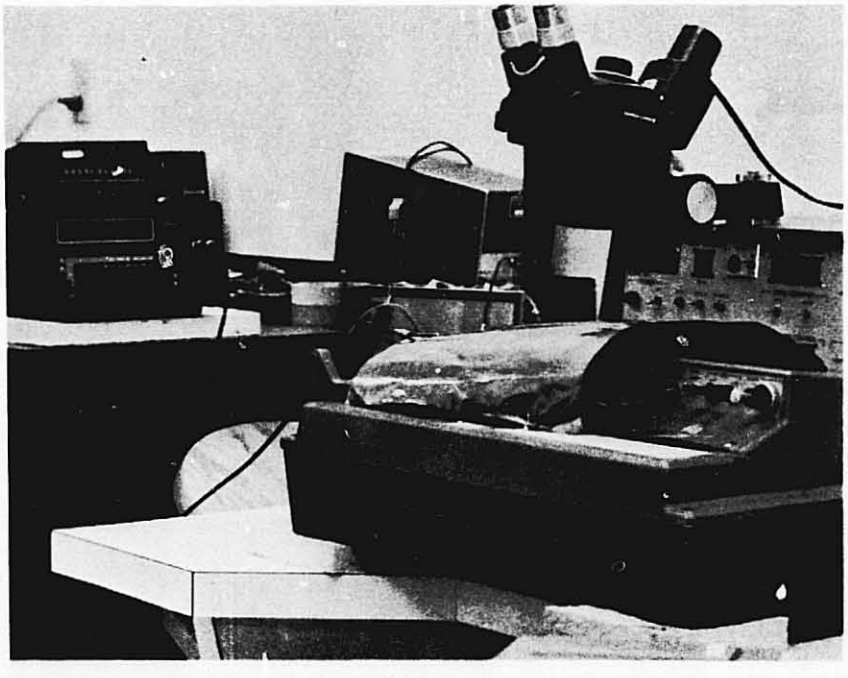


Figure 2. Test set-up for making leakage current measurements. Notice the copper shielding employed to increase precision of measurement.

Figure 3. Test set-up used to monitor via resistance capacitance measurements, short circuit and open circuits for capacitors, cross-overs, and interdigitated fingers.

III. EXPERIMENTAL DATA AND RESULTS

Data and results on an individual dielectric basis and its composite with polyimide are presented together as a group in the same order as the dielectric listing presented in Table 2. Summary results for atmospheric CVD oxide are presented in Tables 3 through 5. It should be noted that this dielectric was annealed at 400°C for 30 minutes in nitrogen prior to taking measurements on it. Thus, for this dielectric (and only this dielectric) data could not be taken on breakdown voltages, leakage currents, via resistances, etc. as a function of anneal temperature and time as was taken for all other dielectrics. Figure 4 (top) presents a profile of via resistance as a function of position across the wafer for 400 and 500°C temperature anneal. The bottom figure represents the behavior of via resistance as a function of anneal temperature (representative data taken on later set of experiments). Figures 5 through 9 represent visual inspections of atmospheric CVD oxide wafers as observed through a microscope. As seen, the deposition of oxide on top of polyimide resulted in severe cracking of this glass layer. Also shown are typical breakdown phenomena on capacitors and cross-over sections of the test-pattern. Figures 10 through 19 illustrate observed results in viewing cross-sections of this dielectric and its polyimide composites using a scanning electron microscope (SEM). Using this analytical technique, thicknesses of the various thin films can be accurately determined, step coverage of the dielectric over first level metal and second level metal over the dielectric can be observed, via formation

and misalignment problems associated with via formation are noted, etc.

Information on low pressure CVD oxides (sometimes referred to as low temperature oxides - LTO) and their composite with polyimides are given in summary Tables 6 through 8 and 14 through 16. The information presented in Tables 9 through 13 represent via resistance data for wafer 2-15 taken at various temperature anneal states. This same data was taken and tabulated for all wafers monitored, but is presented here for this one wafer as an indication of the number of die per wafer monitored (76) and the relative location of these die on the wafer. Based on this data for each wafer, the via resistance vs. position profile curves have been drawn, as shown in Figures 20 through 23. Figure 24 shows a microscope photography of an observed capacitor breakdown location for wafer 7-2, and Figures 25 through 31 present representative SEM analysis for low pressure CVD oxide films and their polyimide composites.

Plasma enhanced oxides and their composites with polyimides are presented in Tables 17 through 23 and associated average via resistance data in Figures 32-through 36. Figures 37 through 42 present microscope observed results associated with plasma deposited oxides and their polyimide composites and Figures 43 through 54 their SEM analysis.

Summary of measured data and visual inspection information for sputtered quartz are presented in Tables 24 through 26 and associated average via resistance data in Figures 55 through 57.

Microscope inspection photographs of sputtered quartz and their polyimide composites are shown in Figures 58 and 59, and related SEM analysis in Figures 60 through 65.

Plasma enchanced nitride summary data is presented in Tables 27 through 29, average via resistance data in Figures 66 through 68, and SEM analysis in Figures 69 through 74.

Lastly, straight polyimide as a dielectric is considered, with summary data presented in Tables 30 through 37 and average via resistance data in Figures 75 through 82. Microscope observations are presented in Figures 83 through 89 and SEM analyses in Figures 90 through 95.

WAFER NUMBER	1-7		DIELECTRIC TYPE	DOPED ATMOSPHERIC OXIDE		
CAPACITANCE (100KHZ)	30.375pf		DIELECTRIC THICKNESS	.979microns		
1st METAL(CO) RESISTANCE	1192ohms		2nd METAL(CO) RESISTANCE	551ohms		

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	.3	750**	N/A	570	160
CROSS-OVER	405	230	N/A	630	470
1st METAL(IF)	55	135	N/A	N/A	N/A
2nd METAL(IF)	80	205	N/A	N/A	N/A
MEASURING VOLTAGE	214.4	142.4	**71.4		

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C
(CO)- CROSS-OVER
(IF)- INTERDIGITATED FINGERS
(NO)- NORMALLY OPEN
OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	1	3	5	1	0
OPENS	0	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VIAS OVER ETCHED, STEEP SIDEWALLS, POOR STEP COVERAGE	BUBBLING IN THE CENTER DIE, OCCATIONAL BREAKDOWNS BETWEEN PADS

Table 3. Measured data and visual inspection summary for wafer MS1-7.

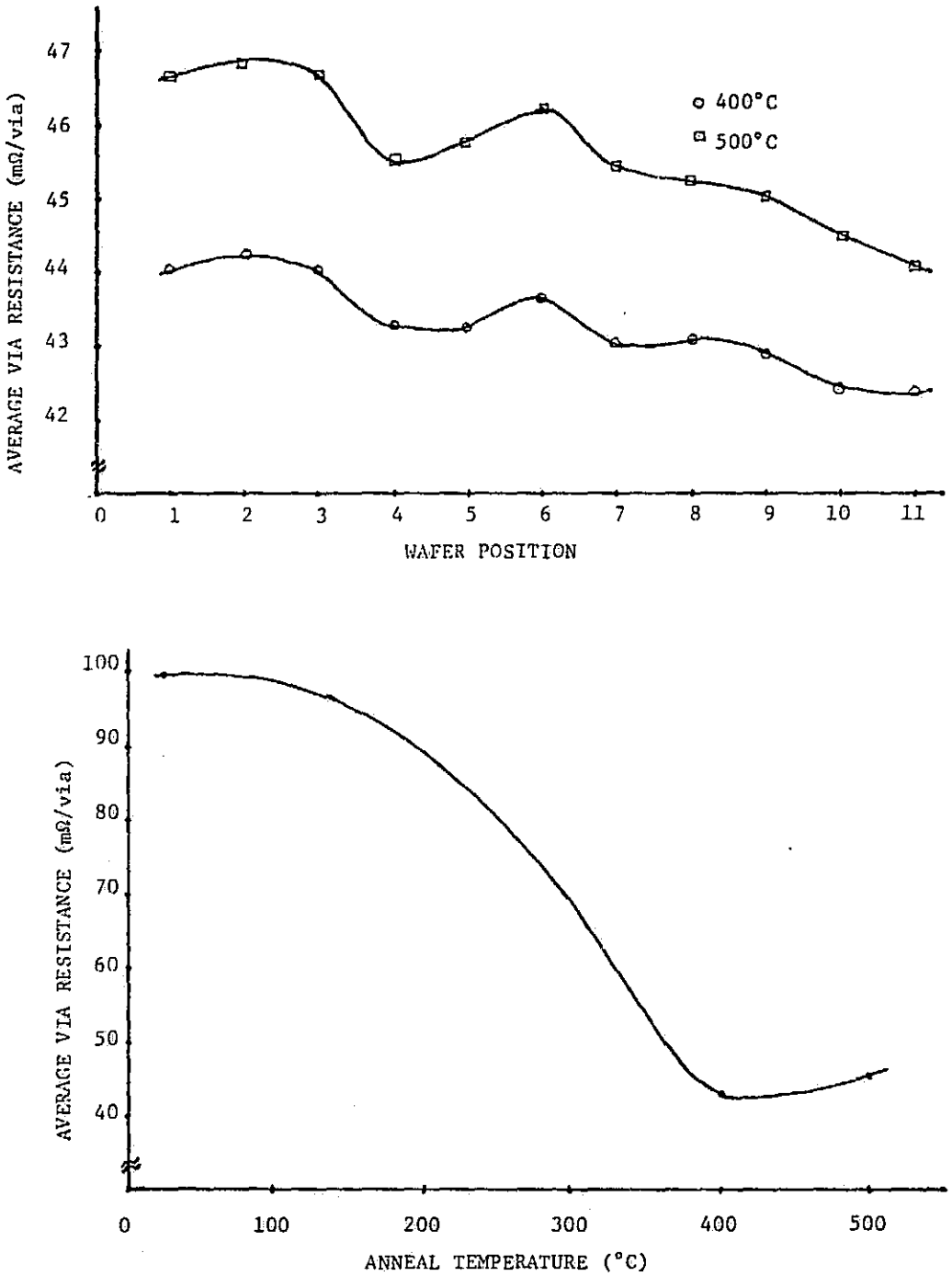


Figure 4. Wafer 1-7. The dielectric consist of 1.0 micron doped atmospheric CVD oxide.

WAFER NUMBER	9-2		DIELECTRIC TYPE	DOPED ATMOS OXIDE + PIQ		
CAPACITANCE (100KHZ)	23.375pf		DIELECTRIC THICKNESS	1.96microns		
1st METAL(CO) RESISTANCE	2633ohms		2nd METAL(CO) RESISTANCE	330ohms		
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	54.9	3.1	590	575	600	*- FINAL TEMPERATURE FOR
CROSS-OVER	1100	170	610	440	575	POLYIMIDE IS 400'C
1st METAL(IF)	180	85	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	560	125	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	200	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R>10Megohm

VIA CHAINS					INTERDIGITATED FINGERS	
1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	0
OPENS	ALL	ALL	ALL	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, LOOKS GOOD	OCCATIONAL BREAKDOWNS BETWEEEN PADS AND ALONG STEPS, NO SIGN OF LIFTING

Table 4. Measured data and visual inspection summary for wafer 9-2.

WAFER NUMBER	9-8		DIELECTRIC TYPE PIQ + DOPED ATMOS OXIDE			
CAPACITANCE (100KHZ)	19pf		DIELECTRIC THICKNESS			1.6microns
1st METAL(CO) RESISTANCE	2784ohms		2nd METAL(CO) RESISTANCE			319ohms
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	5.6	23.6	335	250	355	*- FINAL TEMPERATURE FOR
CROSS-OVER	255	545	455	540	340	POLYIMIDE IS 400'C
1st METAL(IF)	100	280	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	255	470	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	200	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	2	3
OPENS	ALL	ALL	76	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
TOP LAYER OF OXIDE DEVELOPED CRACKS BEFORE 2nd METAL DEPOSITION, METAL IN CRACKS FORMED SHORTS BETWEEN THE TOP OF THE CAPACITOR AND THE CROSS-OVER	NO BUBBLING, BREAKDOWNS OCCURRED AT THE STEPS

Table 5. Measured data and visual inspection summary for wafer 9-8.

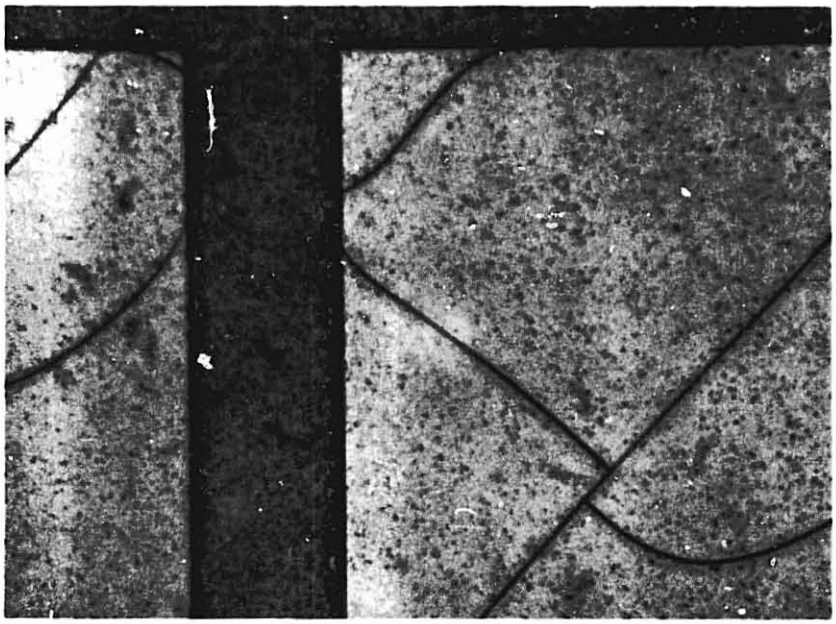


Figure 5. Wafer 9-8. 1μm PIQ plus 4000Å atmospheric CVD SiO_2 Notice cracks in top dielectric.

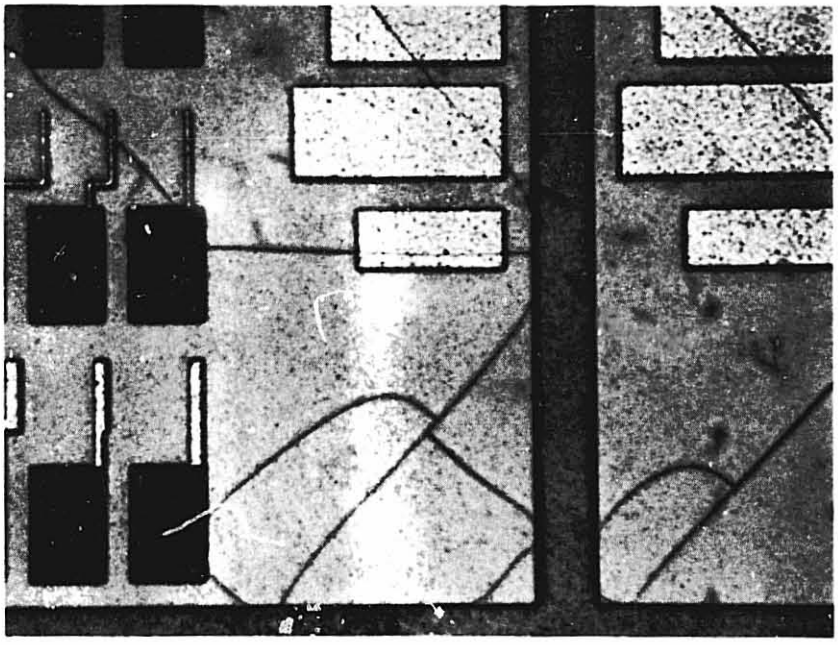


Figure 6. Wafer 9-8. In addition to cracks in CVD oxide, also notice staining of second level metal pads.

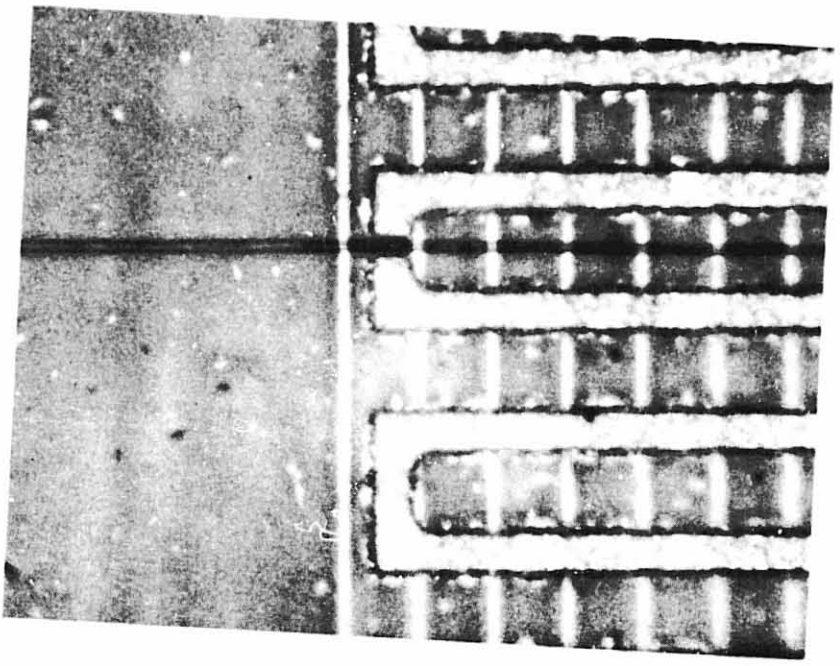


Figure 7. Wafer 9-8. PIQ plus CVD SiO_2. The crack in the top layer dielectric (CVD-SiO_2) is sufficient to cause rupture in second metal cross-over.

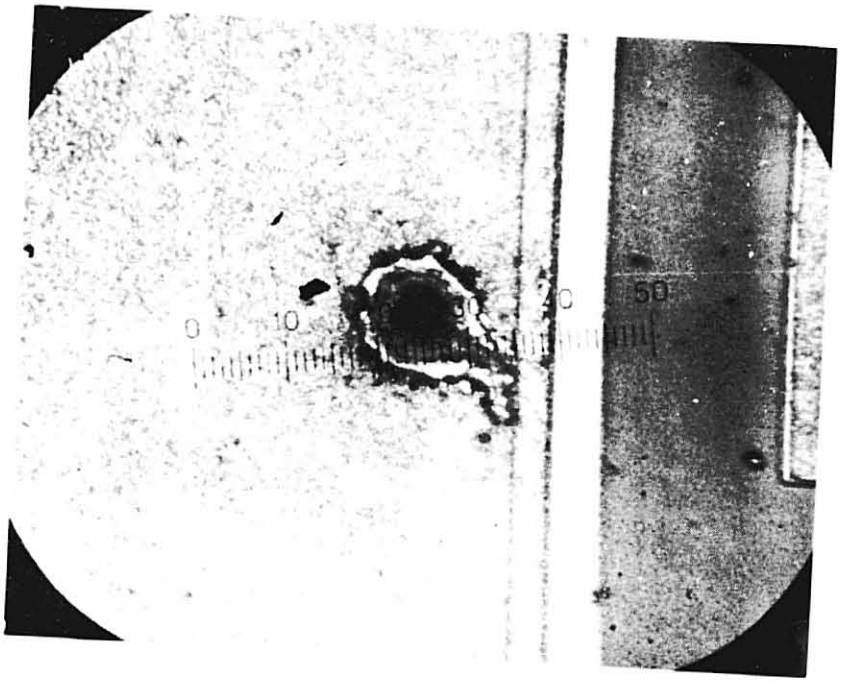


Figure 8. Wafer 1-22. 1µm atmospheric CVD SiO_2. Notice location of capacitor breakdown at 350 volts.

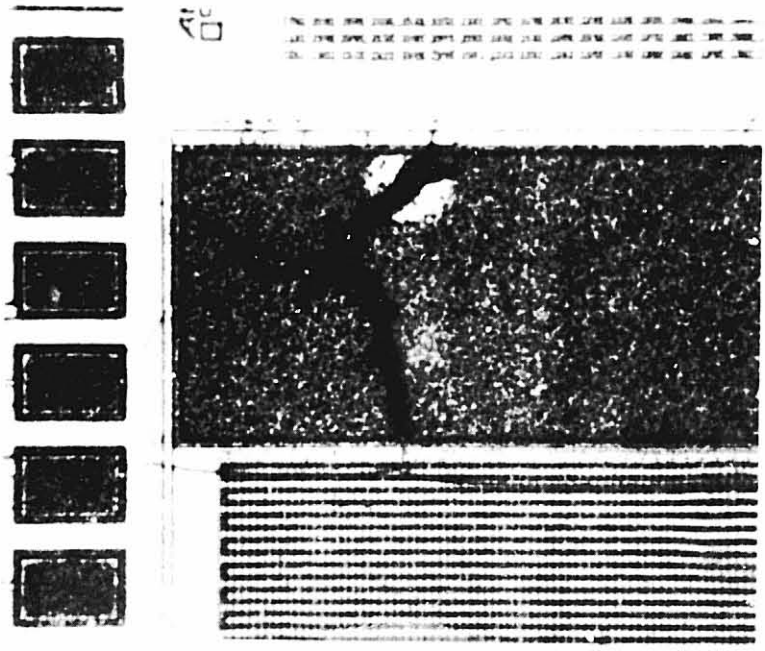


Figure 9. Wafer 9-8. 1μ PIQ plus 4000Å atmospheric CVD SiO_2. Notice that capacitor breakdown in along the crack in top layer oxide.

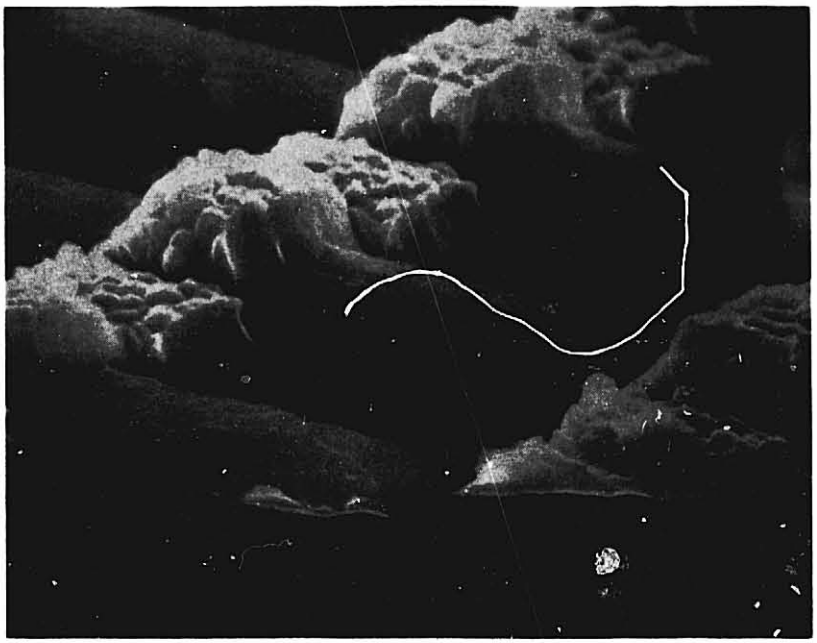


Figure 10. Wafer 1-5, SEM Micrograph of cross-over structure utilizing atmospheric CVD deposited SiO_2 as dielectric of approximately 1 micron thickness. Magnification is 5500X.

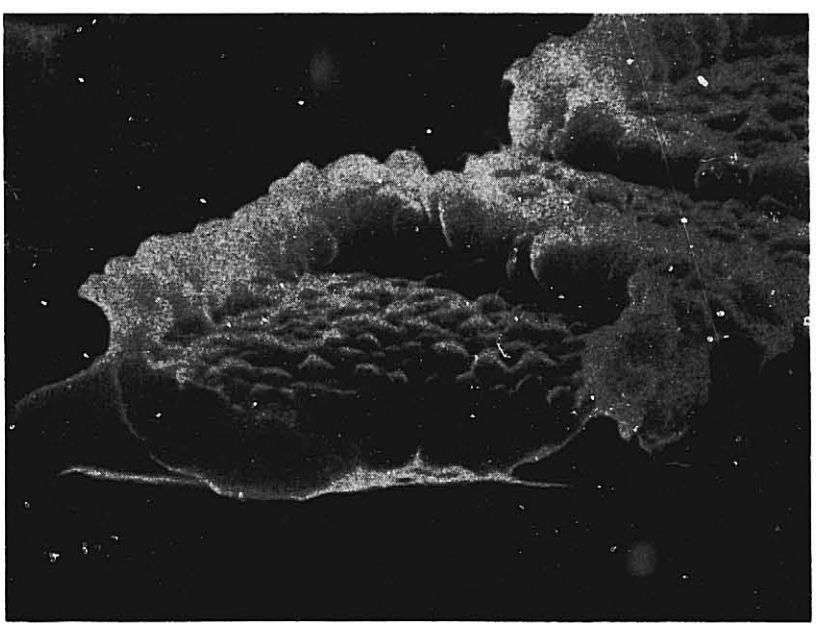


Figure 11. Wafer 1-5, SEM micrograph of via cross-section utilizing 1 micron atmospheric CVD deposited SiO_2 as dielectric. Magnification is 6050X.

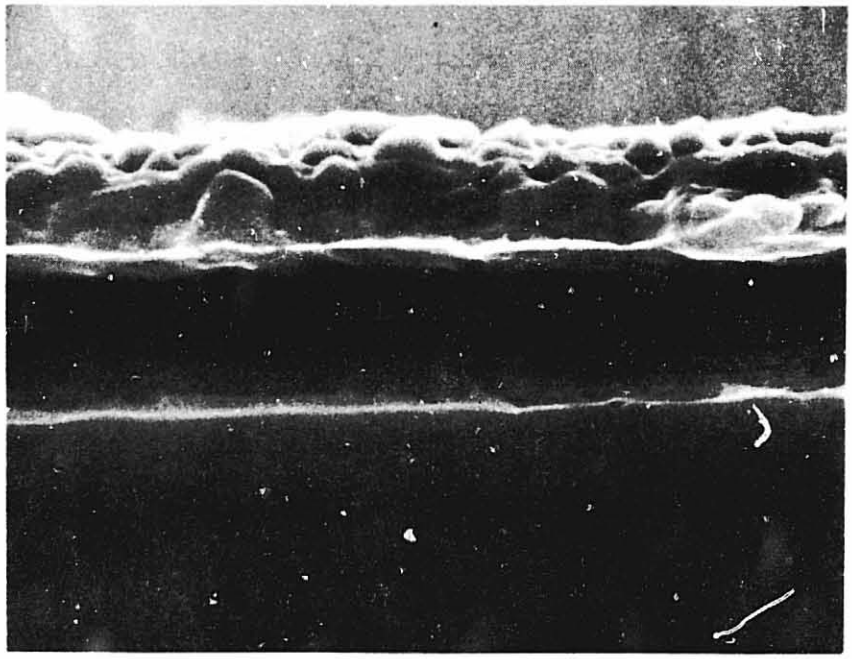


Figure 12. Wafer 1-5, Microslice of large capacitor showing thicknesses of top layer Al/Si, atmospheric CVD SiO_2 and bottom layer Al/Si. Magnification is 8800X. (More accurate thin film thicknesses were obtained from the SEM CRT than that illustrated in this photo.)

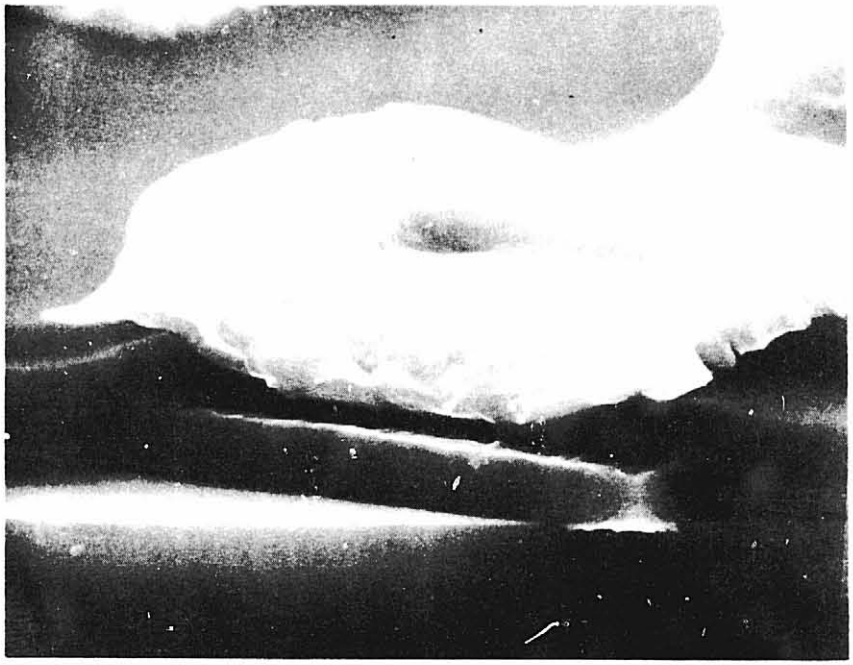


Figure 13. Wafer 9-1, cross-section of a via, dielectric consists of 0.4 μ thick undoped atmospheric CVD SiO_2 (bottom) plus 0.75 μ PIQ-13 (top). Magnification is 6600X.

Figure 14. Cross-over of wafer 9-1, notice planarizing characteristic of polyimide. Magnification is 4400X.

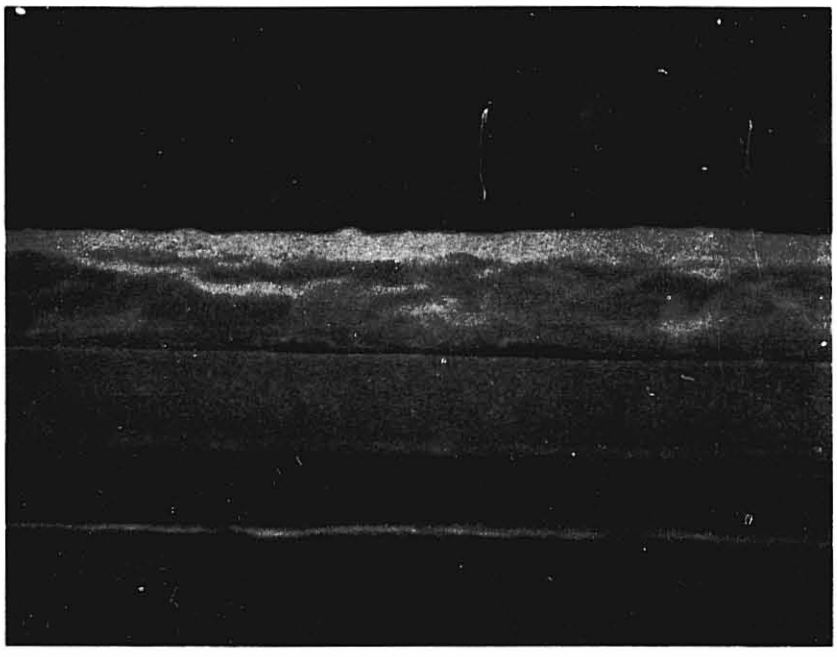


Figure 15. Cross-section of wafer 9-1 showing thickness of top layer Al/Si, PIQ-13, atmospheric CVD SiO_2 and bottom layer Al/Si. Magnification is 8800X.

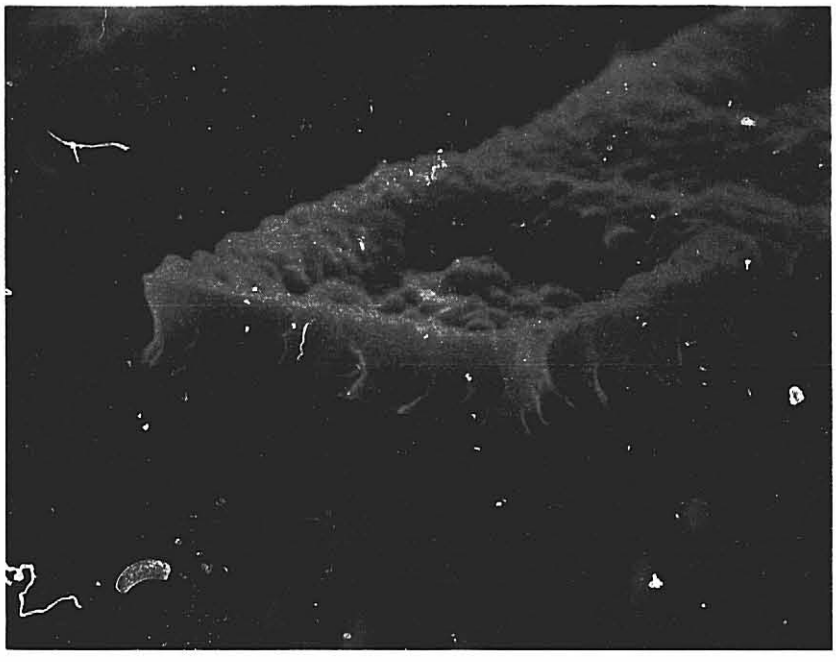


Figure 16. Via of wafer 9-7, dielectric consisting of 0.4 μ atmospheric CVD SiO_2 (top) and approximately 1μ PIQ-13 (bottom). Notice crack in SiO_2 layer. Magnification is 6600X.

Figure 17. Via of wafer 9-7 with top layer Al/Si removed (knocked off in preparing SEM sample). Magnification is 6600X.

Figure 18. Cross-over of wafer 9-7 indicating the two layers of dielectric. Magnification is 6600X.

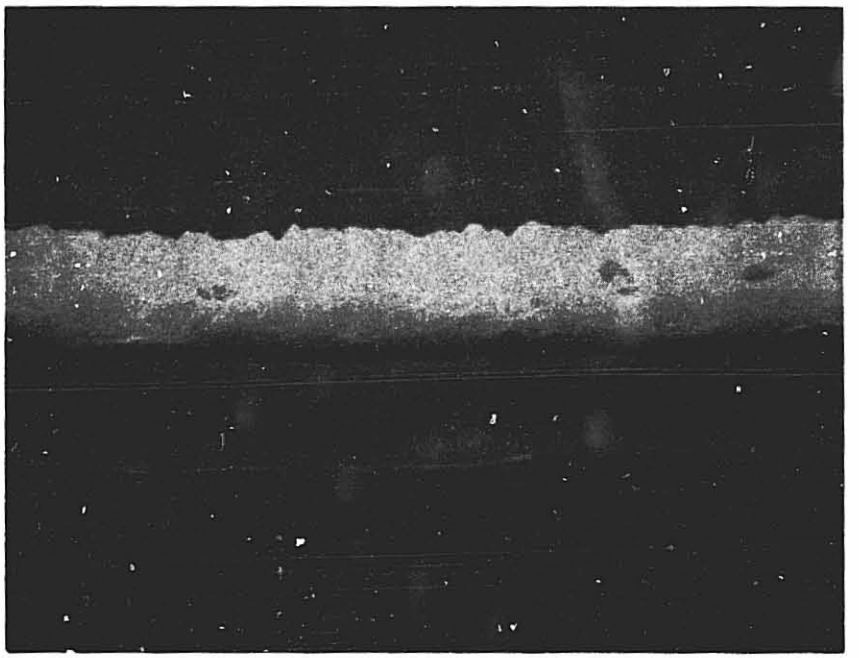


Figure 19. Cross-section of wafer 9-7 showing thickness of top layer Al/Si, atmospheric CVD/SiO_2, polyimide PIQ-13 and bottom layer Al/Si (not shown up here). Magnification is 8800X.

WAFER NUMBER	2-22	DIELECTRIC TYPE	UNDOPED LTO
CAPACITANCE (100KHZ)	35.5pf	DIELECTRIC THICKNESS	1.001microns
1st METAL(CO) RESISTANCE	1455ohms	2nd METAL(CO) RESISTANCE	517ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	.05	.6	610	610	530
CROSS-OVER	255	515	585	420	560
1st METAL(IF)	255	290	N/A	N/A	N/A
2nd METAL(IF)	410	470	N/A	N/A	N/A
MEASURING VOLTAGE	200	314.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C
(CO)- CROSS-OVER
(IF)- INTERDIGITATED FINGERS
(NO)- NORMALLY OPEN
OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	2	0	1	1
OPENS	71	44	63	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VIAS SLIGHTLY OVER ETCHED, STEEP STEPS, NO SIGNS OF LIFTING	MAJORITY OF BREAKDOWNS OCCURED ALONG STEPS

Table 6. Measured data and visual inspection summary for wafer 2-22.

WAFER NUMBER	2-8		DIELECTRIC TYPE	DOPED LTO		
CAPACITANCE (100KHZ)	31.5pf		DIELECTRIC THICKNESS	.998microns		
1st METAL(CO) RESISTANCE	1436ohms		2nd METAL(CO) RESISTANCE	736ohms		
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	35.3	.2	450	640	580	*- FINAL TEMPERATURE FOR
CROSS-OVER	140	425	550	490	520	POLYIMIDE IS 400'C
1st METAL(IF)	140	245	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	245	385	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	214.4	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

VIA CHAINS			INTERDIGITATED FINGERS			
1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS 0	0	0	4	4	2	1
OPENS 71	59	65	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION	
BEFORE ANNEALING	AFTER ANNEALING
VIAS OVER ETCHED, STEEP STEPS, POOR STEP COVERAGE	SMALL AMOUNT OF BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 7. Measured data and visual inspection summary for wafer 2-8.

WAFER NUMBER 2-15 DIELECTRIC TYPE DOPED LTO + PIQ

CAPACITANCE (100KHZ) 19pf DIELECTRIC THICKNESS .951microns

1st METAL(CO) RESISTANCE 1514ohms 2nd METAL(CO) RESISTANCE 301ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	14	.4	555	560	560
CROSS-OVER	180	250	585	530	560
1st METAL(IF)	95	140	N/A	N/A	N/A
2nd METAL(IF)	150	215	N/A	N/A	N/A
MEASURING VOLTAGE	214.4	214.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	1	6	0	1	0	3	6
OPENS	4	2	4	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION AND SLOPE TO SIDEWALLS, GOOD STEP COVERAGE, SLIGHTLY STEEP STEPS	BUBBLING OF CENTER DIE, SOME BREAKDOWNS OCCURED BETWEEN PADS

Table 8. Measured data and visual inspection summary for wafer 2-15.

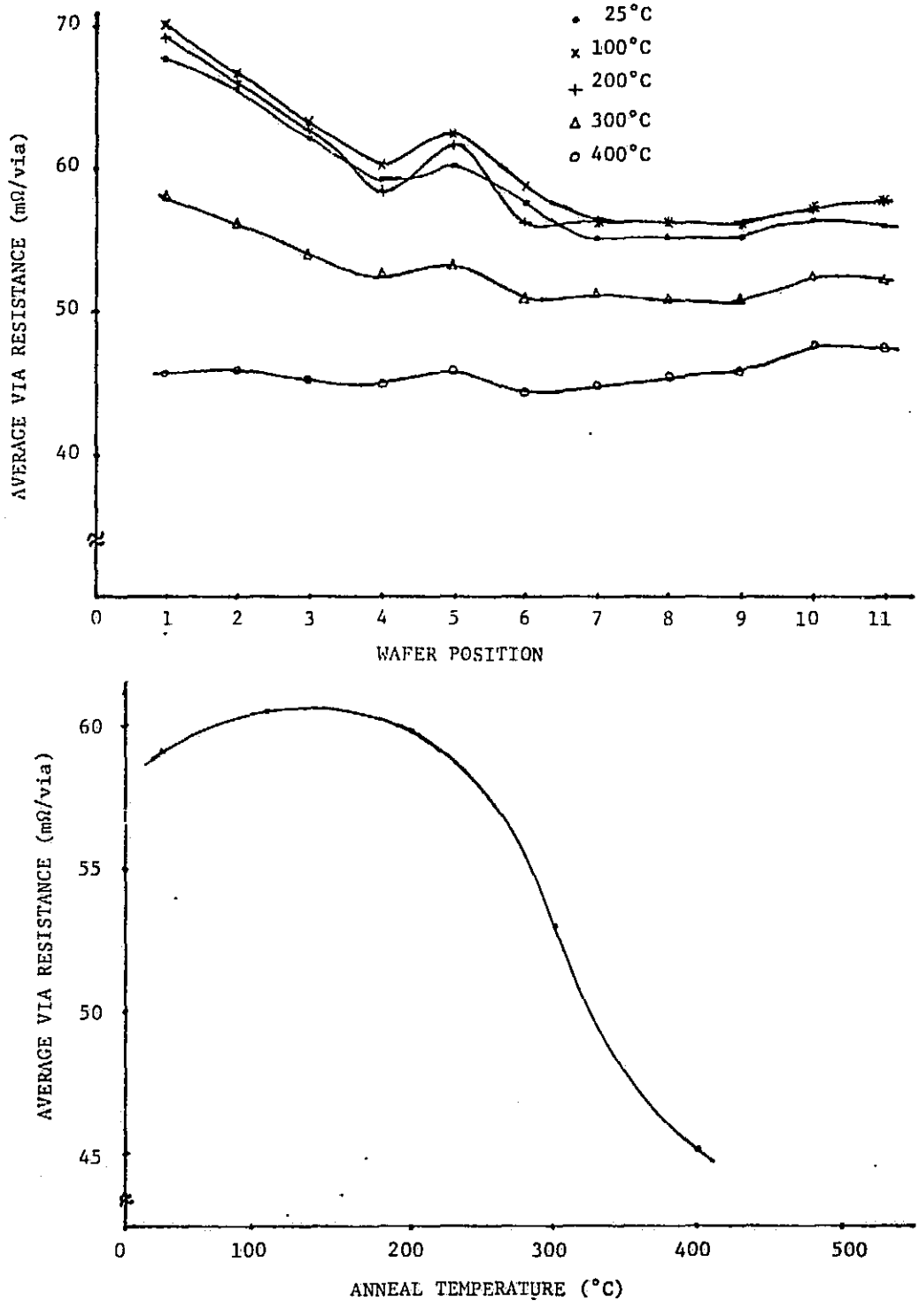


Figure 20. Wafer 2-15. The dielectric consists of 0.25 micron thick low pressure CVD doped oxide (bottom) plus 0.95 microns thick Hitachi PIQ-13 polyimide (top).

POSITION	1	2	3	4	5	6	7	8	9	10	11
1	61.4	59.4	56.4	55.8	56.6	58	56	55.4	54.2	53.5	52.3
2	63.2	62.3	60.1	58.5	57.6	58.7	57.7	56.3	55.5	53.8	53.6
3	65	63.2	61	54	65	58.4	52.1	52.3	54.9	54.8	54.3
4	65.8	63.9	58.9	55.6	60	CENTER	54.9	53.4	53.1	54.4	54.1
5	59.2	65.1	62.8	61.5	59.3	56.6	56.1	54.5	52.8	55.8	56.7
6	77.5	69.7	64.7	62.2	58.7	56.8	54.9	54.3	54.4	55.9	60.6
7	83.3	76	72.5	66.6	64	57.2	54.5	60.5	61.9	66.8	68.5

WAFER	NUMBER	2-15	TEMP.	25 °C	AVERAGE	59.20132	MINIMUM	52.1	MAXIMUN	83.3	
OPENS	0	0	0	0	0	0	0	0	0	0	0
AVERAGE	67.91429	65.65714	62.34286	59.17143	60.17143	57.41667	55.17143	55.24286	55.25714	56.42857	56.01429
MINIMUM	59.3	59.4	56.4	54	56.6	56.6	52.1	52.3	52.8	53.5	52.3
MAXIMUM	83.3	76	72.5	66.6	65	58.7	57.7	60.5	61.9	66.8	68.6

Table 9. Via resistance data for wafer 2-15 as measured before any temperature anneal.

POSITION	1	2	3	4	5	6	7	8	9	10	11
1	62.5	60.4	57.4	56.8	57.6	59.5	56.9	56.3	55.2	54.5	53.4
2	64.1	63.2	61	59.4	58.5	59.7	58.7	57.3	56.5	54.8	54.6
3	65.9	64.1	61.9	54.8	66.5	58.8	53	52.2	55.9	55.8	55.2
4	66.9	64.7	59.9	56.8	69.9	CENTER	56.1	54.4	54.1	55.4	55.1
5	78	66.8	63.7	62.4	60.1	57.8	56.9	55.4	52.7	56.7	57.6
6	78.4	70.8	65.6	63.1	59.6	57.9	55.7	55.2	55.3	56.8	66
7	84.1	76.9	73.4	68.1	65.4	58.1	55.6	62.1	63	68	61.6

WAFER	NUMBER	2-15	TEMP.	100 °C	AVERAGE	60.40026	MINIMUM	52.2	MAXIMUN	84.1	
OPENS	0	0	0	0	0	0	0	0	0	0	0
AVERAGE	70.27143	66.7	63.27143	60.2	62.51429	58.63333	56.12857	56.12857	56.1	57.42857	57.44286
MINIMUM	62.5	60.4	57.4	54.8	57.6	57.8	53	52.2	52.7	54.5	53.4
MAXIMUM	84.1	76.9	73.4	68.1	69.9	59.7	58.7	62.1	63	68	66

Table 10. Via resistance data for wafer 2-15 as measured after a 30 minute 100°C temperature anneal in nitrogen.

POSITION	1	2	3	4	5	6	7	8	9	10	11
1	62	60.1	57.2	56.7	57.5	46.1	56.9	56.4	55.3	54.5	53.5
2	63.6	65.9	60.7	59.2	58.4	59.5	58.7	57.2	56.5	54.8	54.7
3	65.2	63.5	61.6	54.7	65.8	58.7	52.8	52.1	55.9	55.9	55.8
4	66.1	63.9	59.4	56.4	60.1	CENTER	56.1	54.5	54.1	55.4	55.1
5	68.8	65.9	63	61	59.9	57.6	56.9	55.5	52.6	56.7	57.5
6	76.5	69.5	64.7	62.4	59.4	57.7	55.6	55.1	55.3	56.8	65.4
7	81.6	75	71.9	60	64	57.7	55.2	61.8	63	68.2	61.5

WAFER	NUMBER	2-15	TEMP.	200 'C	AVERAGE	59.86447	MINIMUM	46.1	MAXIMUN	81.6	
OPENS	0	0	0	0	0	0	0	0	0	0	0
AVERAGE	69.11429	66.25714	62.64286	58.62857	61.87143	56.21667	56.02857	56.08571	56.1	57.47143	57.57143
MINIMUM	62	60.1	57.2	54.7	57.5	46.1	52.8	52.1	52.6	54.5	53.5
MAXIMUM	81.6	75	71.9	62.4	68.1	59.5	58.7	61.8	63	68.2	65.4

Table 11. Via resistance data for wafer 2-15 measured after an additional 30 minute 200°C temperature anneal in nitrogen.

POSITION	1	2	3	4	5	6	7	8	9	10	11
1	54.7	53.8	51.9	51.8	52.3	42.1	52.1	51.8	51	50.6	49.6
2	55.4	55.2	54.2	53.3	52.8	53.7	56.7	52.2	51.9	50.6	50.4
3	56.2	55.6	54.5	48.9	55.2	55.4	47.9	46.8	51.1	51.2	50.6
4	56.3	55.2	52.1	50.1	54.7	CENTER	51.1	49.7	49.3	50.4	50.1
5	57.5	56.2	54.5	54.2	52.9	51.6	51.1	50.1	47.1	51.1	51.5
6	62.2	58.3	55.1	54.1	52.2	51.4	49.8	49.5	49.7	51	56.7
7	64.7	61	56.3	56.4	53.3	50.7	49	55.5	56.5	61.9	55.5

WAFER	NUMBER	2-15	TEMP.	300 'C	AVERAGE	53.01711	MINIMUM	42.1	MAXIMUN	64.7	
OPENS	0	0	0	0	0	0	0	0	0	0	0
AVERAGE	58.14286	56.47143	54.08571	52.71429	53.34286	50.81667	51.1	50.8	50.94286	52.4	52.05714
MINIMUM	54.7	53.8	51.9	48.9	52.2	42.1	47.9	46.8	47.1	50.4	49.6
MAXIMUM	64.7	61	56.3	56.4	55.2	55.4	56.7	55.5	56.5	61.9	56.7

Table 12. Via resistance data for wafer 2-15 measured after an additional 30 minutes 300°C anneal in nitrogen.

POSITION	1	2	3	4	5	6	7	8	9	10	11
1	45.6	45.2	44.8	44.9	44.8	37.1	44.8	44.9	44.7	44.8	44.5
2	45.2	46.3	45.2	45.1	44.8	45	47	44.8	45.1	44.9	44.9
3	45.1	45.2	45.3	41.1	46.9	45.2	40.7	41	45	45	44.6
4	45.1	45.1	44.2	43.6	48.6	CENTER	45.2	44.5	44.1	44.6	44.6
5	45.8	45.4	45.4	45.8	45.4	47.8	46.8	45.2	42.7	46.7	46
6	46.4	46.8	45.5	45.6	44.9	46	44.8	44.4	44.8	46.6	51.5
7	46.3	46.9	46.2	48.3	46.1	44.4	44.6	52	53.5	60	53.6

WAFER	NUMBER	2-15	TEMP.	400 'C	AVERAGE	45.66843	MINIMUM	37.1	MAXIMUN	60	
OPENS	0	0	0	0	0	0	0	0	0	0	0
AVERAGE	45.64286	45.84286	45.22857	44.91429	45.92857	44.25	44.77143	45.25714	45.7	47.51429	47.1
MINIMUM	45.1	45.1	44.2	41.1	44.8	37.1	40.7	41	42.7	44.6	44.5
MAXIMUM	46.4	46.9	46.2	48.3	48.6	47.8	47	52	53.5	60	53.6

Table 13. Via resistance data for wafer 2-15 measured after an additional 30 minutes 400°C anneal in nitrogen.

WAFER NUMBER 2-2 DIELECTRIC TYPE UNDOPED LTC♦ PIQ

CAPACITANCE (100KHZ) 18pf DIELECTRIC THICKNESS .953microns

1st METAL(CO) RESISTANCE 1363ohms 2nd METAL(CO) RESISTANCE 305ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	2.5	.2	620	630	580
CROSS-OVER	125	265	660	595	575
1st METAL(IF)	80	170	N/A	N/A	N/A
2nd METAL(IF)	125	250	N/A	N/A	N/A

MEASURING VOLTAGE 214.4 214.4

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R>10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	0	4
OPENS	1	1	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
SLOPED VIA SIDEWALLS, GOOD STEP COVERAGE, NO SIGNS OF LIFTING	BUBBLING IN THE CENTER DIE, SOME BREAKDOWNS BETWEEN PADS

Table 14. Measured data and visual inspection summary for wafer 2-2.

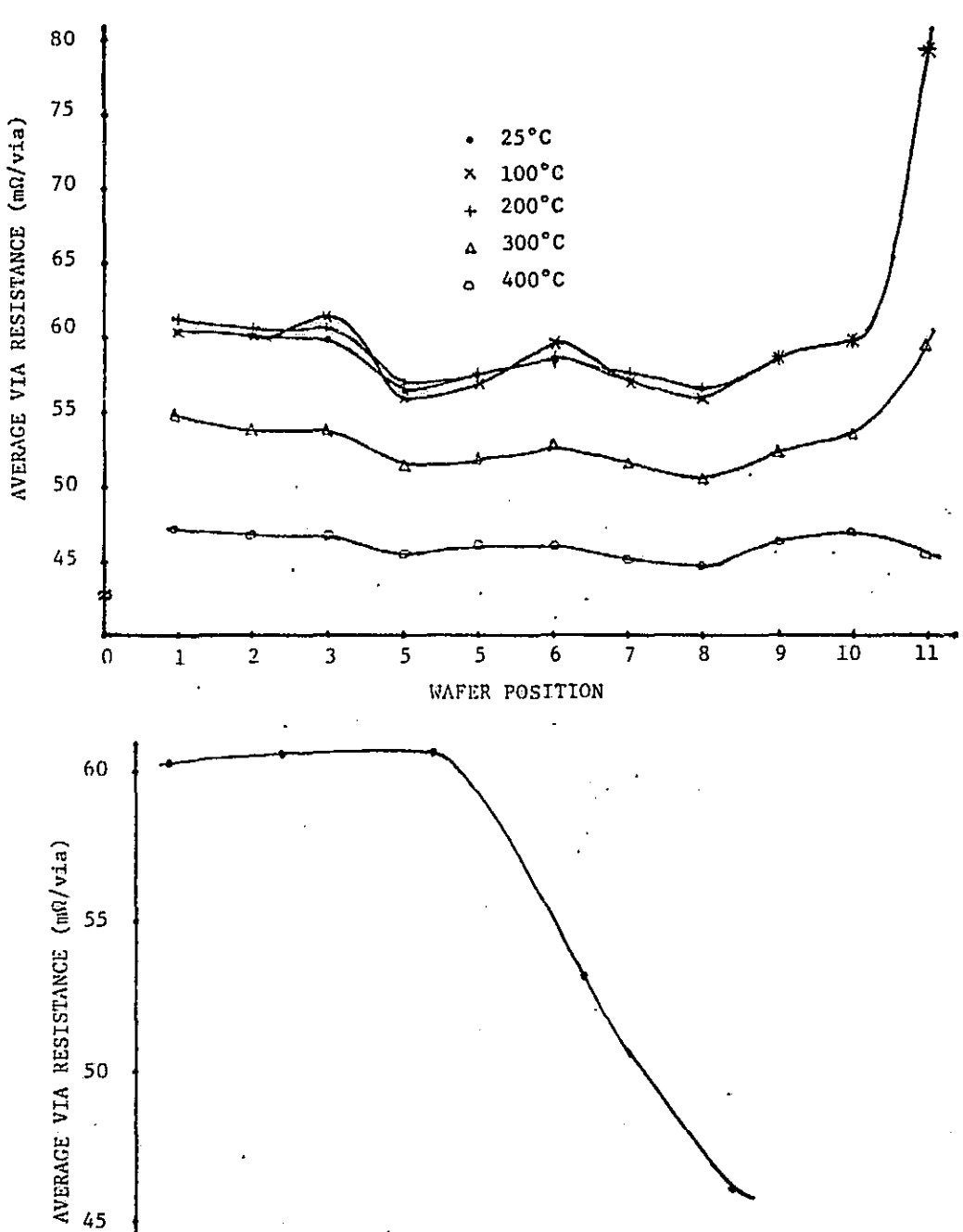


Figure 21. Wafer 2-2. The dielectric consist of 0.25 microns undoped low pressure CVD oxide (bottom) plus 1.05 microns Hitachi PIQ-13 polyimide (top).

WAFER NUMBER 7-2 DIELECTRIC TYPE PIQ + DOPED LTO

CAPACITANCE (100KHZ) 26.875pf DIELECTRIC THICKNESS .931microns

1st METAL(CO) RESISTANCE 1048ohms 2nd METAL(CO) RESISTANCE 341ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	6.4	9.1	480	480	355
CROSS-OVER	230	350	400	495	345
1st METAL(IF)	110	110	N/A	N/A	N/A
2nd METAL(IF)	165	155	N/A	N/A	N/A
MEASURING VOLTAGE	142.8	142.8			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R>10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	2	1	0	1	2	0	1
OPENS	3	3	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION AND SIDEWALL SLOPE, GOOD STEP COVERAGE	BUBBLING IN CENTER DIE, NO SIGN ON 2nd METAL LIFTING

Table 15. Summary of measured data and visual inspection for wafer 7-2.

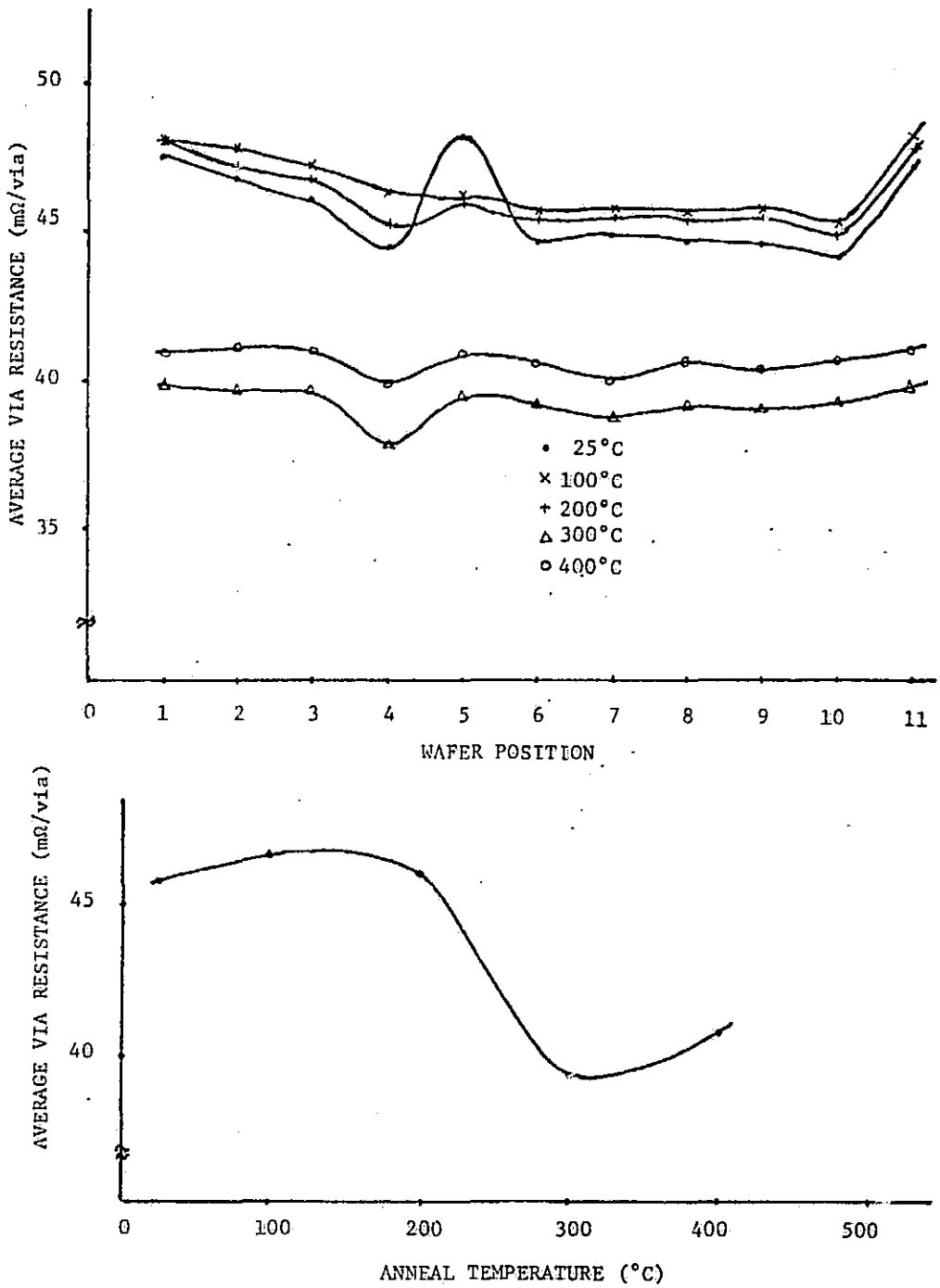


Figure 22. Wafer 7-2. The dielectric consist of 0.65 microns thick layer of Hitachi PIQ-13 (bottom) plus a 0.25 micron thick low pressure CVD doped oxide (top).

WAFER NUMBER	7-13		DIELECTRIC TYPE	PIQ + UNDOPED LTO		
CAPACITANCE (100KHZ)	29.875pf		DIELECTRIC THICKNESS	.953microns		
1st METAL(CO) RESISTANCE	1173ohms		2nd METAL(CO) RESISTANCE	360ohms		
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	.7	1.8	510	470	330	*- FINAL TEMPERATURE FOR
CROSS-OVER	85	330	490	430	345	POLYIMIDE IS 400'C OTHERS 500'C
1st METAL(IF)	50	80	N/A	N/A	N/A	(CO)- CROSS-OVER (IF)- INTERDIGITATED
2nd METAL(IF)	75	150	N/A	N/A	N/A	FINGERS (NO)- NORMALLY OPEN
MEASURING VOLTAGE	142.8	142.8				OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1040	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	3	0	0	2	2	0	1
OPENS	0	2	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, GOOD STEP COVERAGE, NO SIGNS OF LIFTING	BUBBLING IN THE CENTER DIE, SOME BREAKDOWNS OCCURING ALONG STEPS

Table 16. Summary of measured data and visual inspection for wafer 7-13.

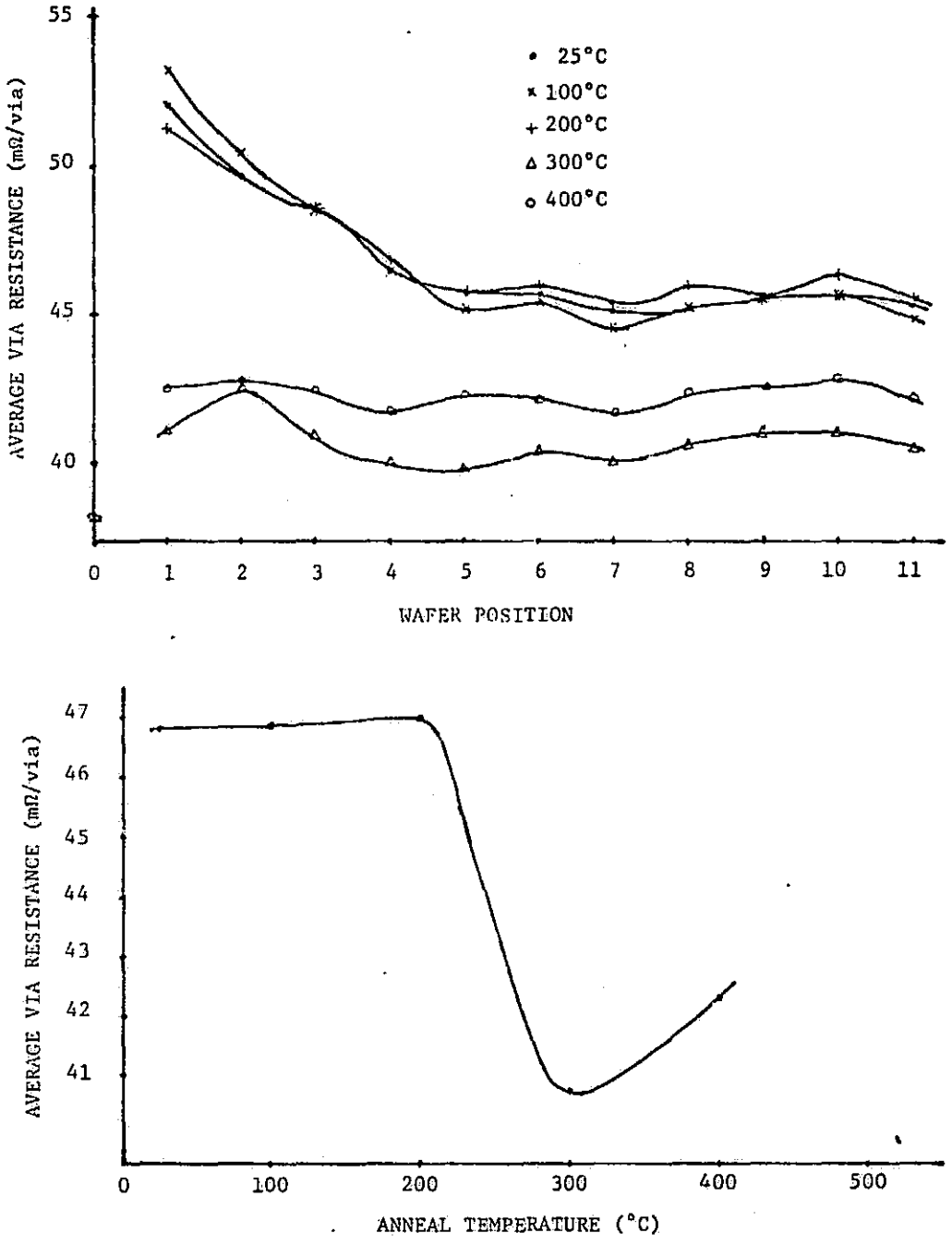


Figure 23. Wafer 7-13. The dielectric consists of 0.55 microns Hitachi PIQ-13 (bottom) plus 0.25 microns low pressure CVD undoped oxide (top).

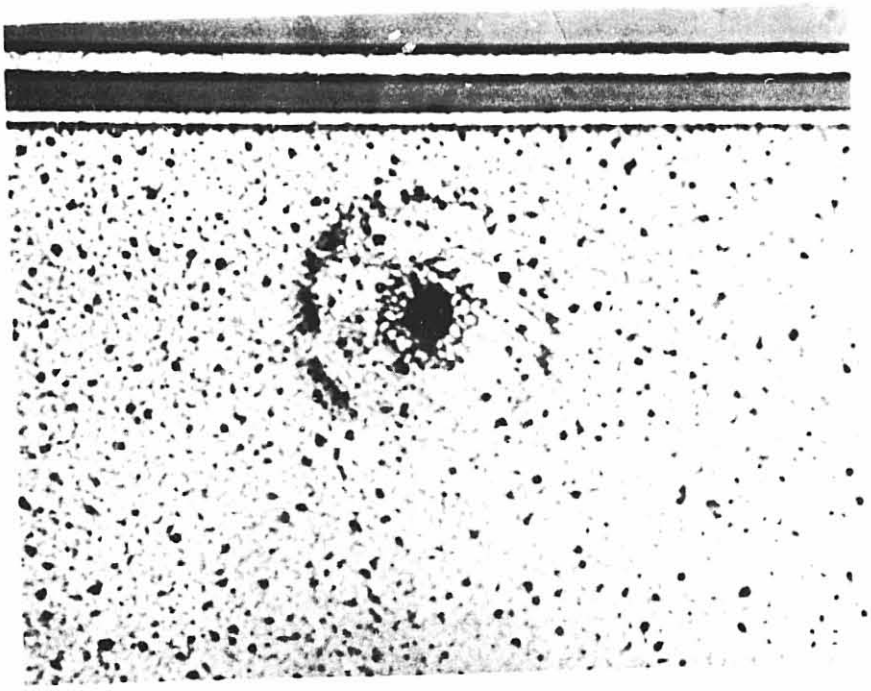


Figure 24. Wafer 7-2. 1μ PIQ plus 2500Å doped LPCVD SiO_2. Notice location of capacitor breakdown.

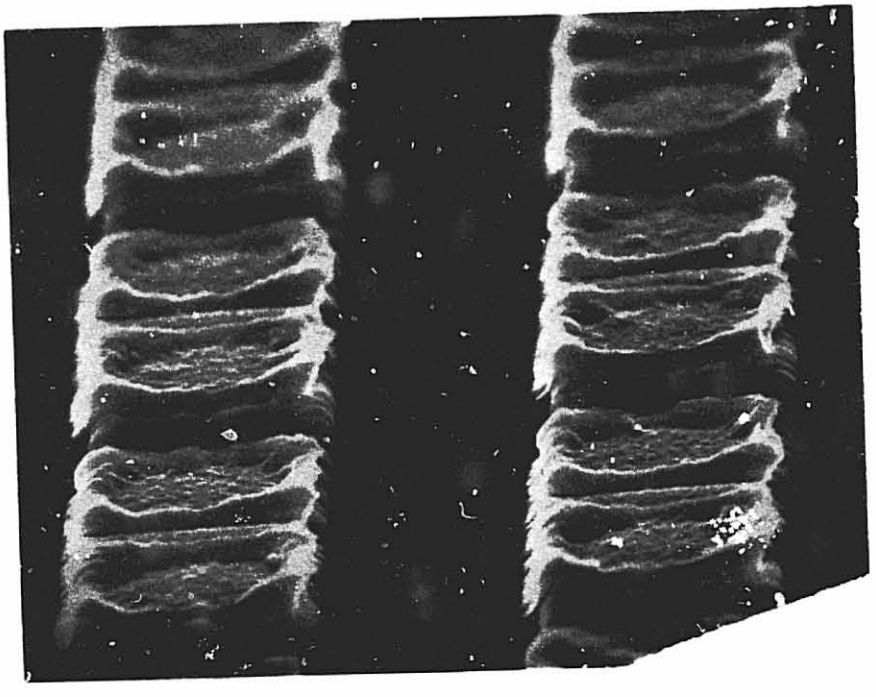


Figure 25. Via's of wafer 2-21, dielectric consist of approximately 1 μ undoped LPCVD SiO_2. Magnification is 2750X.

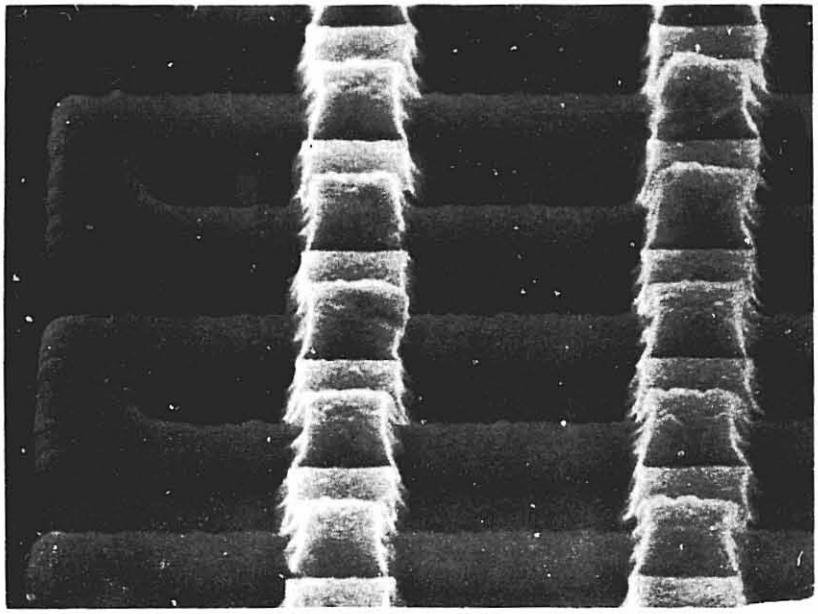


Figure 26. Cross-over of wafer 2-21 illustrating step-coverage. Magnification is 2750X.

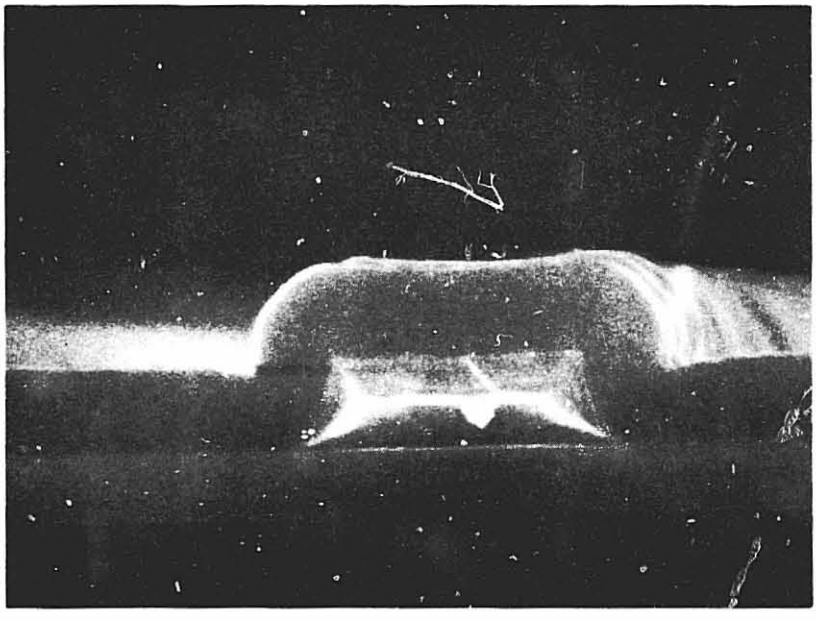


Figure 27. Step coverage of first level metal for wafer 2-21. Magnification is 11,000X.

Figure 28. Via's of wafer 2-13, dielectric consist of doped LPCVD SiO_2 (bottom) and polyimide PIQ-13 (top). Magnification is 5500X.

Figure 29. Cross-over for wafer 2-13. Magnification is 7700X.

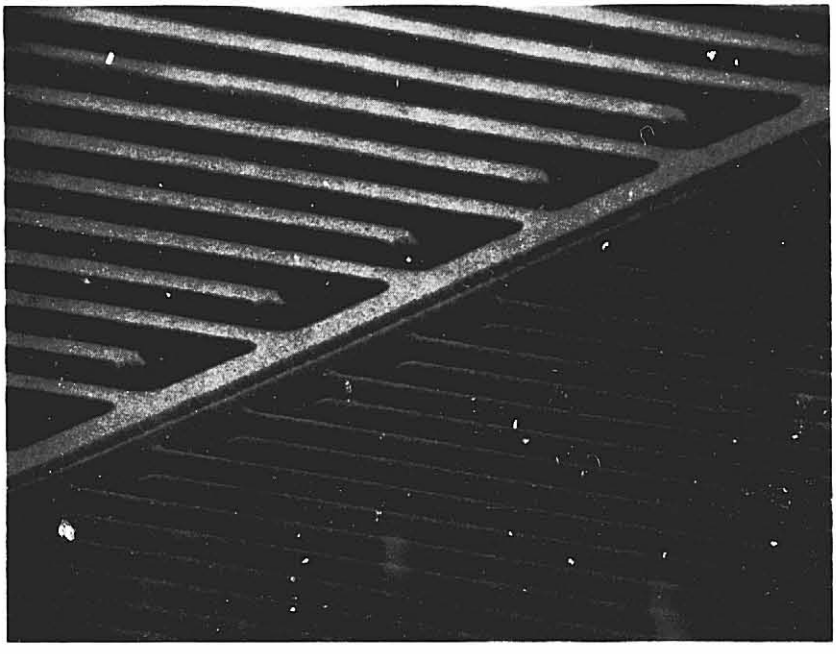


Figure 30. A view of top and bottom layer interdigitated finger layout for wafer 2-13. Magnification is 1100X.

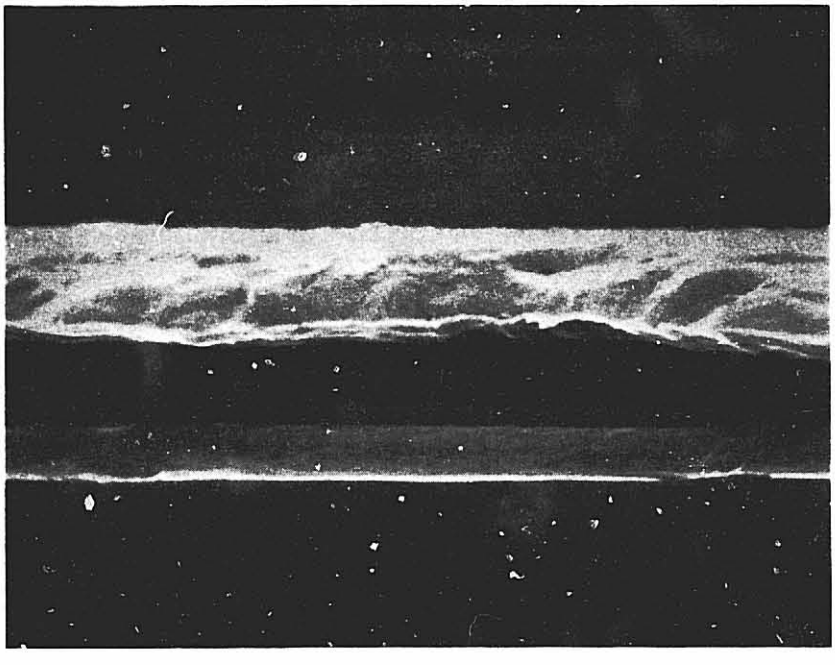


Figure 31. Cross-section of big capacitor for wafer 2-13 illustrating top layer Al/Si, polyimide PIQ, thin layer of LPCVD SiO_2 and bottom layer of Al/Si.

WAFER NUMBER	3-23		DIELECTRIC TYPE	DOPED PLASMA OXIDE		
CAPACITANCE (100KHZ)	35pf		DIELECTRIC THICKNESS	.993microns		
1st METAL(CO) RESISTANCE	1621ohms		2nd METAL(CO) RESISTANCE	456ohms		
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	1	.1	510	555	540	*- FINAL TEMPERATURE FOR
CROSS-OVER	370	450	460	310	540	POLYIMIDE IS 400'C
1st METAL(IF)	230	260	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	380	445	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	214.4	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1060	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	4	4	5	2	34	0	0
OPENS	1	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
OVEN ETCHED VIAS, POOR STEP COVERAGE, STEEP STEPS	NO BUBBLING, BREAKDOWNS OCCURRED AT STEPS

Table 17. Summary of measured data and visual inspection for wafer 3-23.

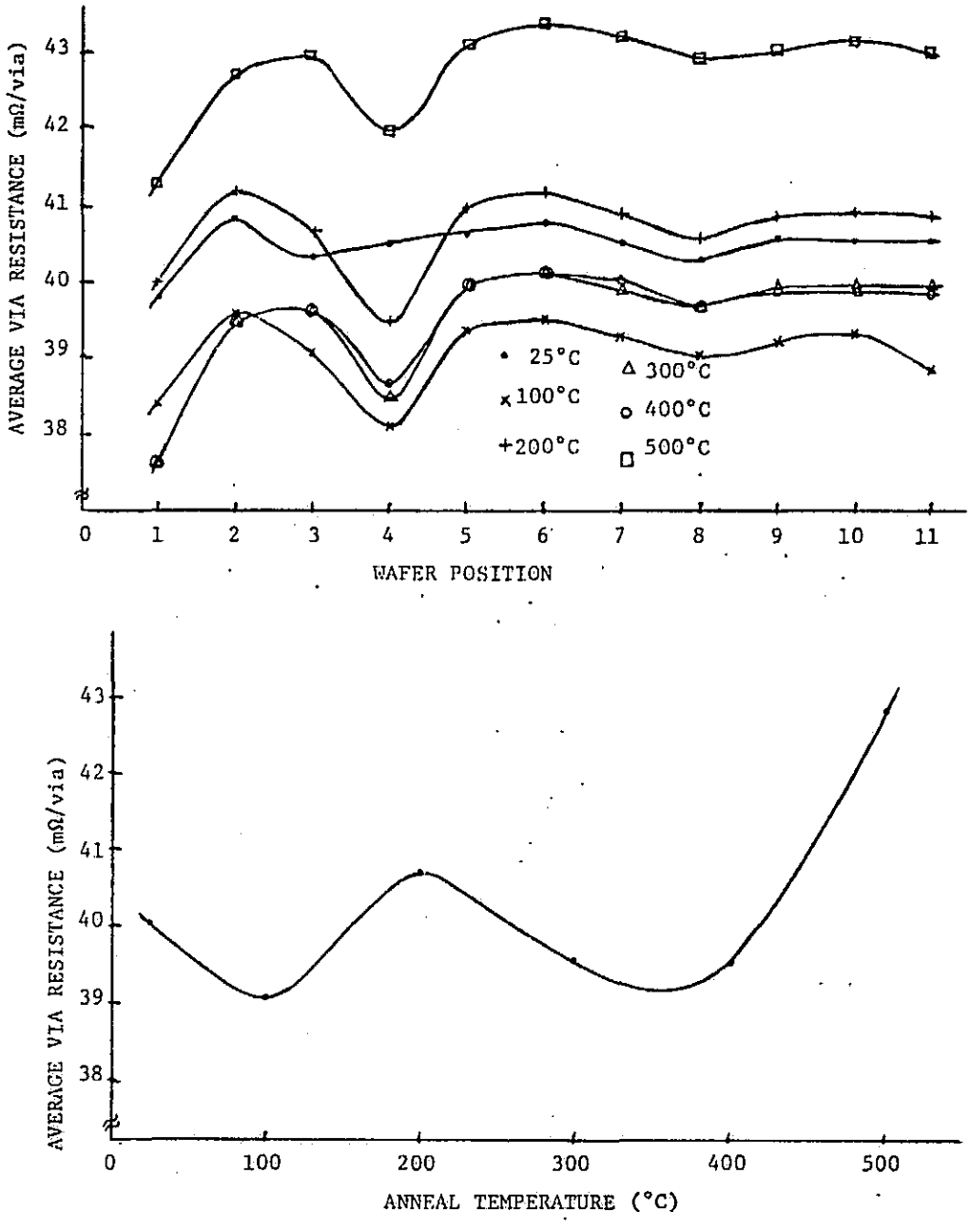


Figure 32. Wafer 3-23. The dielectric consist of 0.95 microns doped plasma enhanced oxide.

WAFER NUMBER 3-9 DIELECTRIC TYPE UNDOPED PLASMA OXIDE

CAPACITANCE (100KHZ) 25.3pf DIELECTRIC THICKNESS 1.039microns

1st METAL(CO) RESISTANCE 2109ohms 2nd METAL(CO) RESISTANCE 454ohms

	LEAKAGE CURRENT(pa)		BREBREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	300 'C	FINAL *	
CAPACITOR	7	.05	350	590	540	*- FINAL TEMPERATURE FOR
CROSS-OVER	215	300	820	480	460	POLYIMIDE IS 400'C
1st METAL(IF)	275	170	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	320	260	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.8	142.8				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1040	400	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	2	0	0	23	31	0	1
OPENS	14	10	8	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VIAS OVER ETCHED, VERY SLOPED SIDE WALLS, STEEP STEPS, POOR STEP COVERAGE, OVER ETCHING AND UNDER ETCHING IN THE SAME LOCATIONS	NO BUBBLING, BREAKDOWNS OCCURRED AT STEPS

Table 18. Summary of measured data and visual inspection for wafer 3-9.

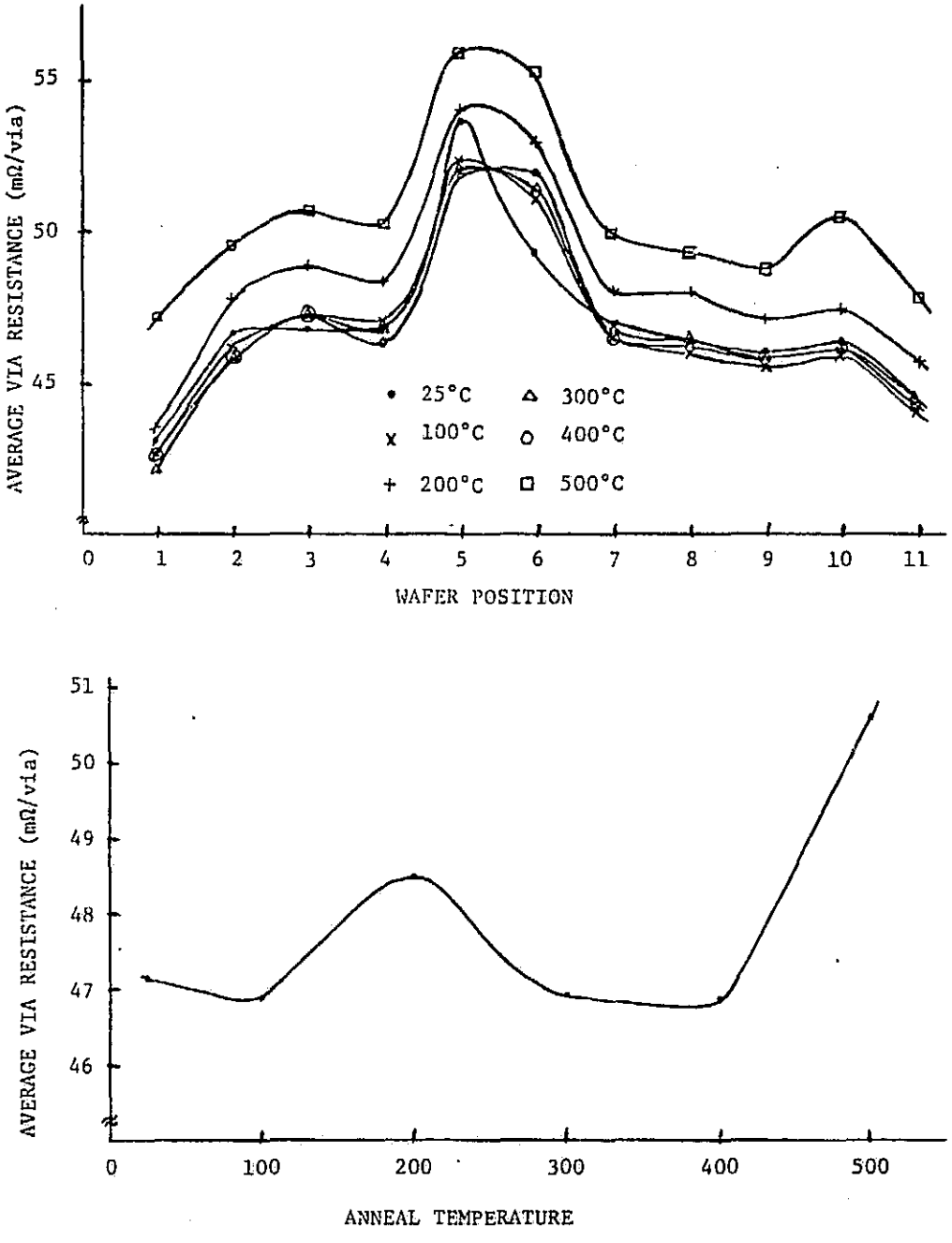


Figure 33. Wafer 3-9. The dielectric consist of 1.1 microns of undoped plasma enhanced oxide.

WAFER NUMBER	3-6		DIELECTRIC TYPE DOPED PLASMA OXIDE + PIQ			
CAPACITANCE (100KHZ)	22.75pf		DIELECTRIC THICKNESS			.71microns
1st METAL(CO) RESISTANCE	1303ohms		2nd METAL(CO) RESISTANCE			286ohms
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	3.5	.1	545	565	530	*- FINAL TEMPERATURE FOR
CROSS-OVER	310	265	465	480	495	POLYIMIDE IS 400'C
1st METAL(IF)	95	155	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	145	220	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.8	142.8				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

VIA CHAINS			INTERDIGITATED FINGERS			
1000	400	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS 0	0	0	1	1	2	1
OPENS 2	0	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, SLOPED SIDE WALLS, GOOD STEP COVERAGE	BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 19. Summary of measured data and visual inspection for wafer 3-6.

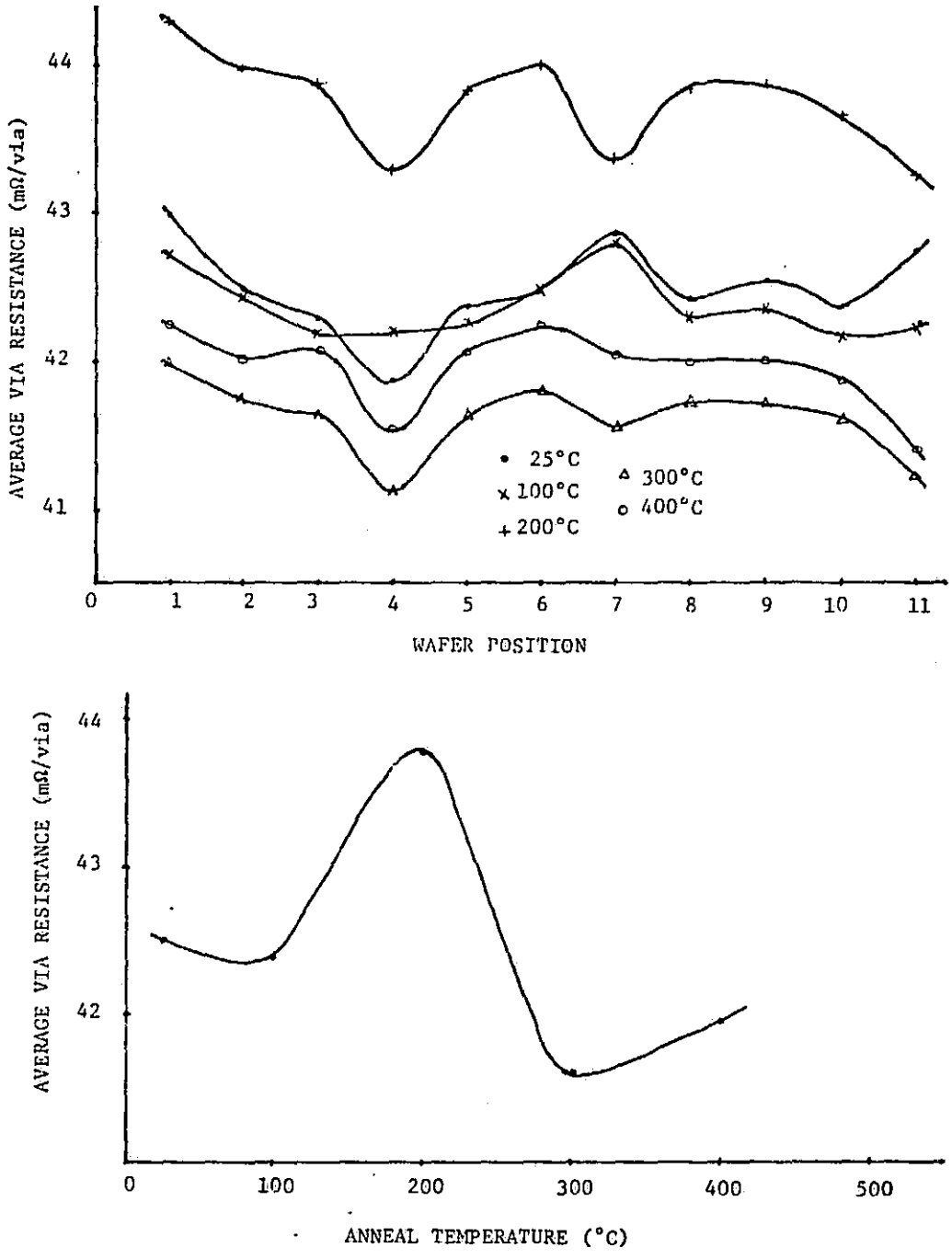


Figure 34. Wafer 3-6. The dielectric consist of 0.25 microns doped plasma enhanced oxide (bottom) plus 0.85 microns Hitachi PIQ-13 (top).

WAFER NUMBER 7-25 DIELECTRIC TYPE UNDOPED PLASMA OXIDE(LFE) + PIQ

CAPACITANCE (100KHZ) 22pf DIELECTRIC THICKNESS .938microns

1st METAL(CO) RESISTANCE 1098ohms 2nd METAL(CO) RESISTANCE 342ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	9.8	1.7	540	575	600
CROSS-OVER	160	290	545	530	530
1st METAL(IF)	90	160	N/A	N/A	N/A
2nd METAL(IF)	145	250	N/A	N/A	N/A
MEASURING VOLTAGE	214.4	214.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

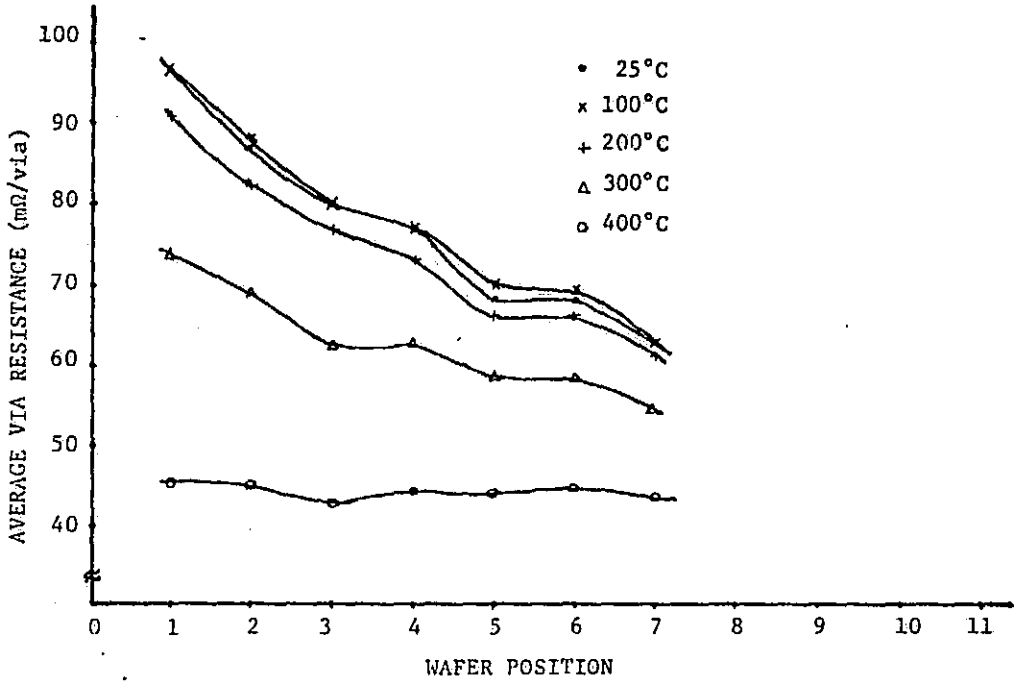
OPEN- R>10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1040	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	1	0	1	2	1	0	1
OPENS	1	4	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION AND SIDEWALL SLOPE, GOOD STEP COVERAGE	BUBBLING IN THE CENTER DIE, OCCATIONAL BREAKDOWNS BETWEEN PADS

Table 20. Summary of measured data and visual inspection for wafer 7-25.



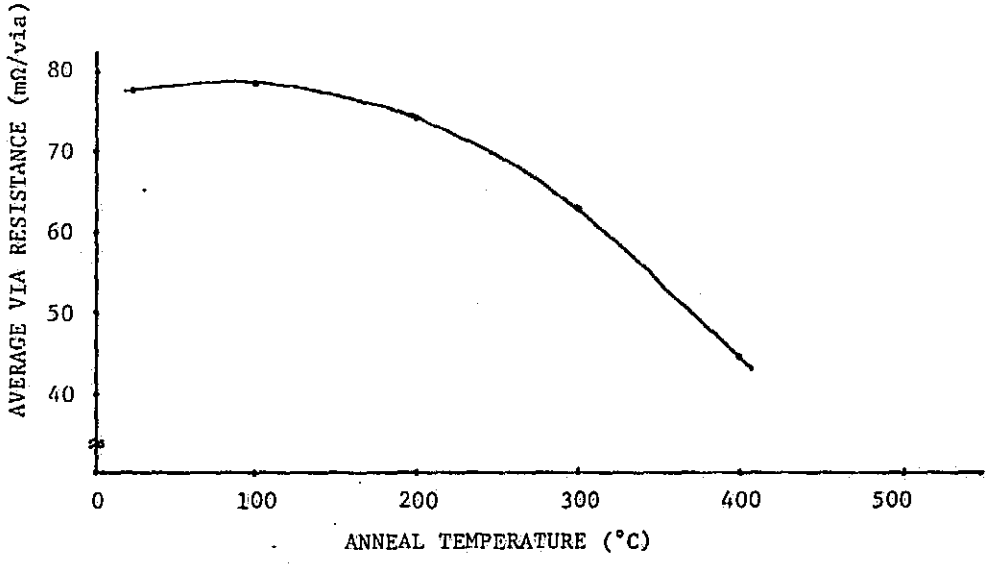


Figure 35. Wafer 7-25. The dielectric consist of 0.26 microns undoped plasma enhanced oxide (bottom) plus 0.84 micron Hitachi PIQ-13 (top).

WAFER NUMBER 7-15 DIELECTRIC TYPE PIQ + DOPED PLASMA OXIDE

CAPACITANCE (100KHZ) 30.875pf DIELECTRIC THICKNESS .68microns

1st METAL(CO) RESISTANCE 1211ohms 2nd METAL(CO) RESISTANCE N/A ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	26	2385	300	440	330	*- FINAL TEMPERATURE FOR
CROSS-OVER	210	10000	520	480	400	POLYIMIDE IS 400'C
1st METAL(IF)	380	700	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	170	650	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.8	142.8				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	6	2	1	2
OPENS	ALL	ALL	ALL	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GROSSLY OVER ETCHED VIAS, GOOD STEP COVERAGE, SOME SIGNS OF LIFTING	BUBBLING IN THE CENTER DIE, SOME SIGNS OF LIFTING

Table 21. Summary of measured data and visual inspection for wafer 7-15.

WAFER NUMBER 7-14 DIELECTRIC TYPE PIQ + UNDOPED PLASMA OXIDE

CAPACITANCE (100KHZ) 29.5pf DIELECTRIC THICKNESS .90microns

1st METAL(CO) RESISTANCE 1286ohms 2nd METAL(CO) RESISTANCE 342ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	100	17.2	500	460	310
CROSS-OVER	---	680	---	---	390
1st METAL(IF)	255	335	N/A	N/A	N/A
2nd METAL(IF)	---	600	N/A	N/A	N/A
MEASURING VOLTAGE	200	214.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1080	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	2	0	1	5
OPENS	ALL	ALL	ALL	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
SLIGHTLY ROUNDED VIAS, LIFT-OFF IN SOME AREAS, ENTIRE TOP LAYER OF METAL OF THE CENTER DIE	2nd METAL LIFTING EVERYWHERE, LOOKS BAD

Table 22. Summary of measured data and visual inspection for wafer 7-14.

WAFER NUMBER 3-25 DIELECTRIC TYPE DOPED PLASMA OXIDE (LFE)

CAPACITANCE (100KHZ) 38pf DIELECTRIC THICKNESS 1microns

1st METAL(CO) RESISTANCE 1272ohms 2nd METAL(CO) RESISTANCE 330ohms

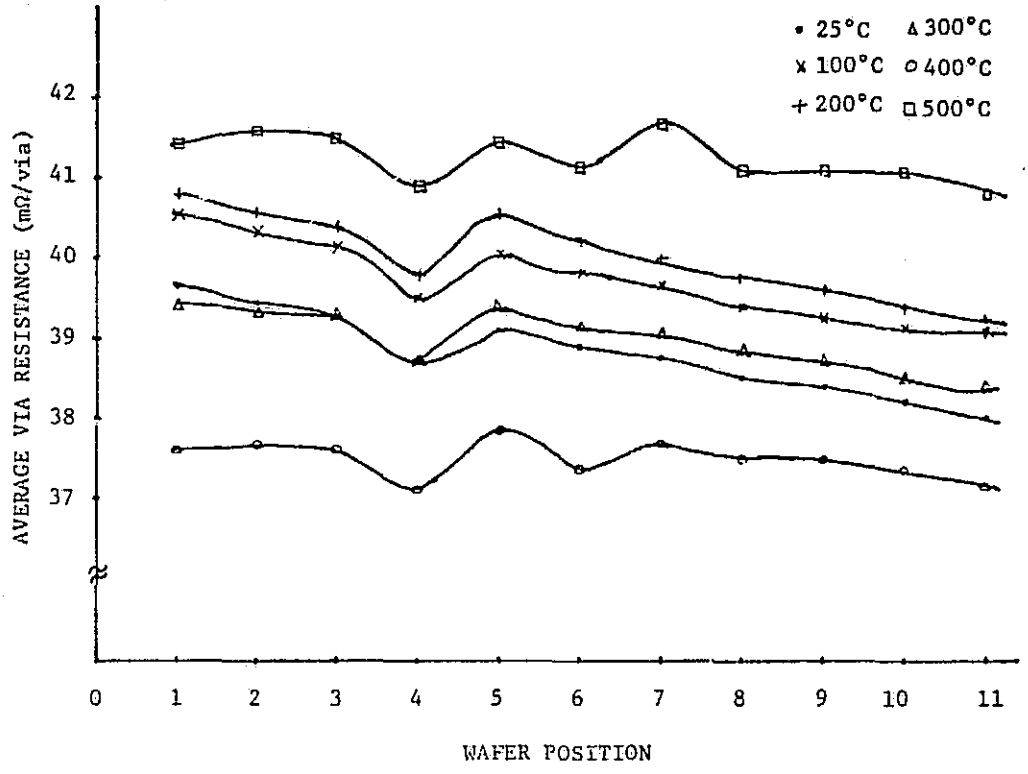
	LEAKAGE CURRENT(pa)		BREBREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	11.8	3.6	500	260	355	*- FINAL TEMPERATURE FOR
CROSS-OVER	---	200	---	440	480	POLYIMIDE IS 400'C
1st METAL(IF)	150	110	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	290	310	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	214.4	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	1	0	0	27	55	1	1
OPENS	1	2	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
SLIGHTLY OVER ETCHED VIAS, POOR STEP COVERAGE, POSSIBLE BREAKS IN CAPACITOR AND CROSS-OVER	BUBBLING IN CENTER DIE AND TOP PLATE OF CAPACITOR, BREAKDOWNS OCCURED AT STEPS

Table 23. Summary of measured data and visual inspection for wafer 3-25.



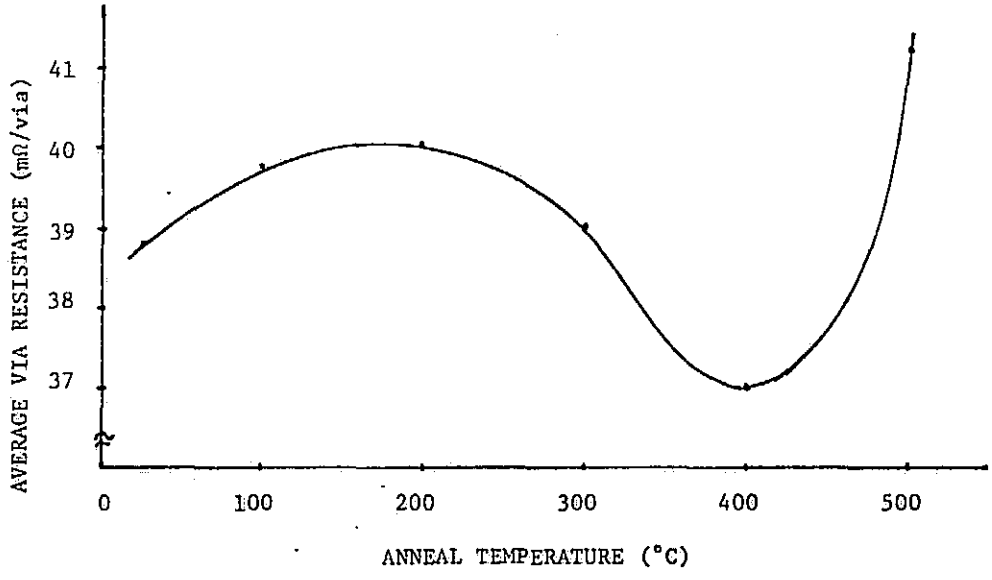


Figure 36. Wafer 3-25. The dielectric consists of 0.8 micron undoped plasma enhanced oxide.

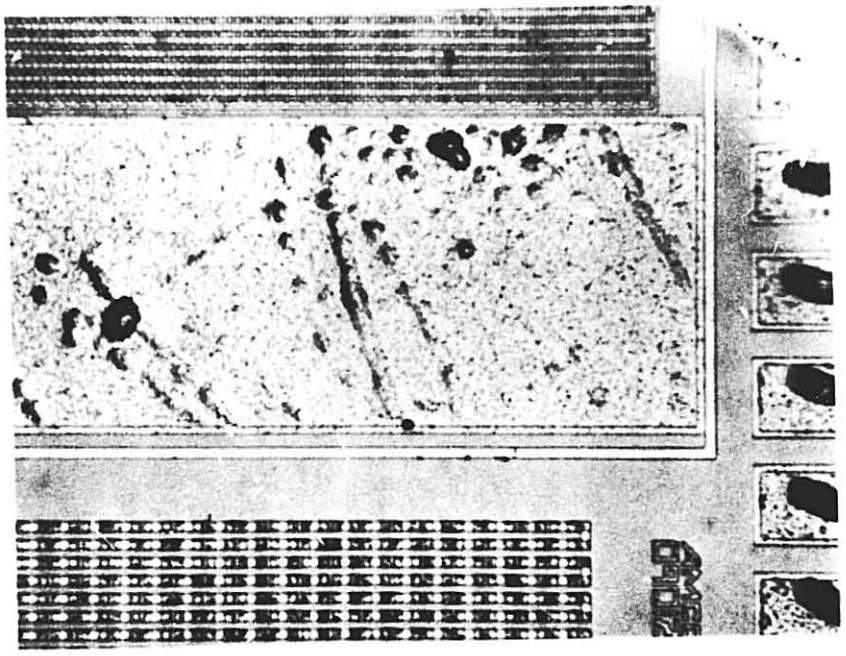


Figure 37. Wafer 3-25. 1μm doped plasma enhanced SiO_2 (from LFE). Notice bubbles in second level metal of big capacitor.

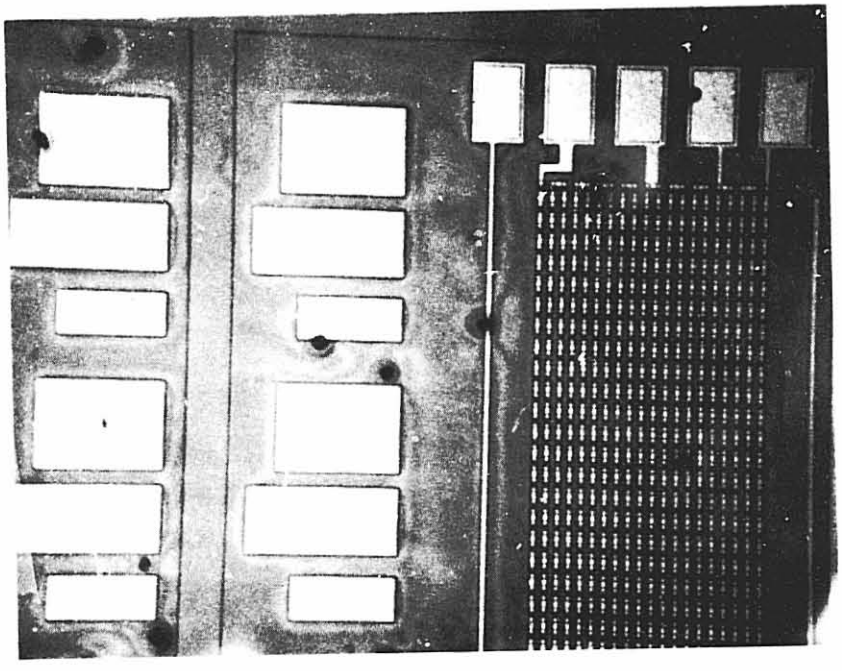


Figure 38. On a few of the doped plasma enhanced SiO_2 obtained from Pacific Western, particulate count was large. These particles could be removed by the scrubber, however, this left voids in the oxide rendering shorts between metal layers.

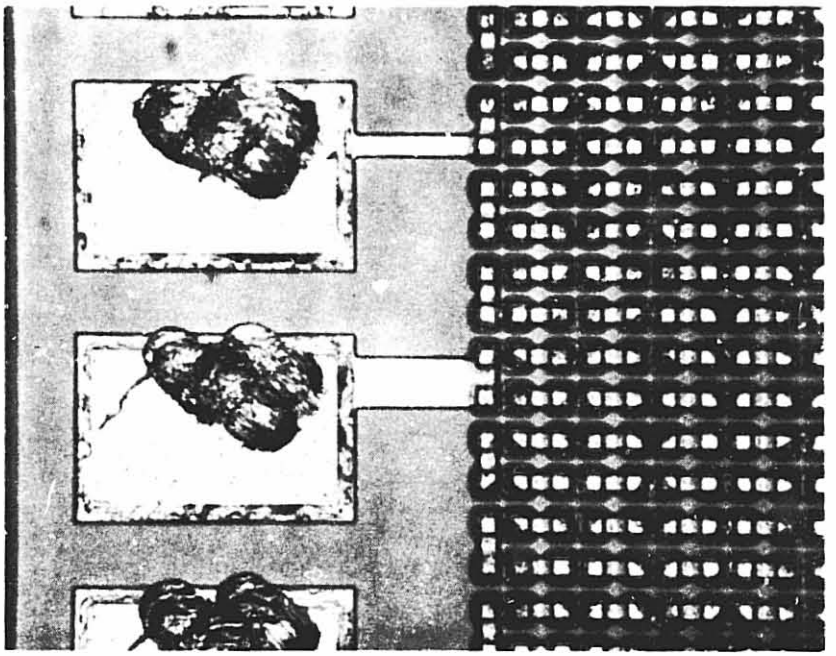


Figure 39. Wafer 3-9. 1μm undoped plasma enhanced SiO_2. Notice over-etching of via's and residue left in the pads.

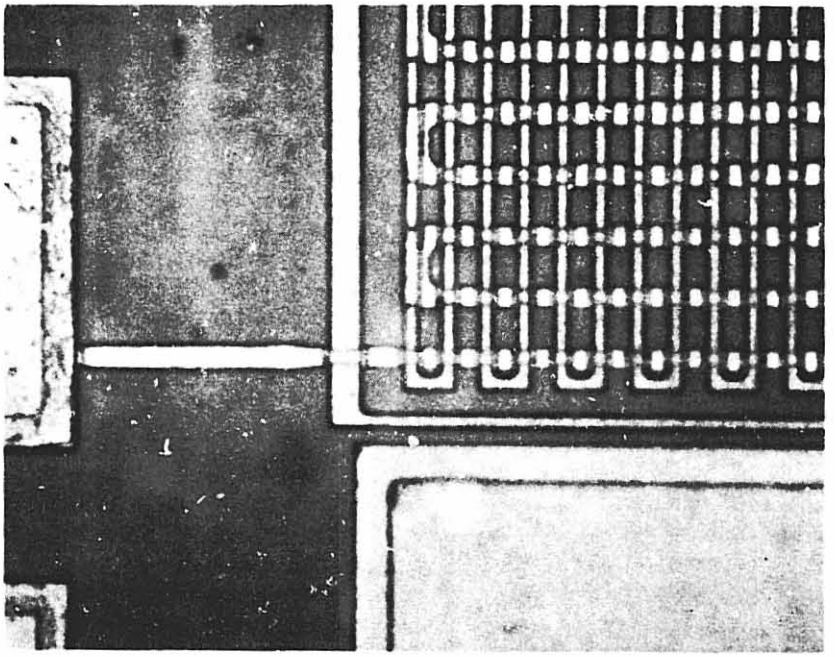


Figure 40. Wafer 3-9. Notice the poor step-coverage at the cross-overs (very narrow metal).

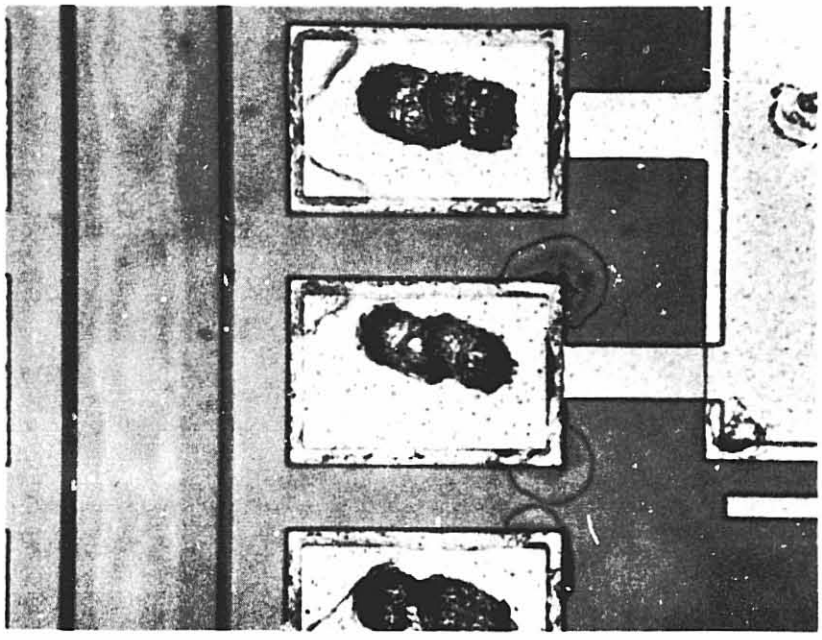


Figure 41. Wafer 3-9. 1μm undoped plasma enhanced SiO_2. Notice overetch in some pads (middle) and residue in others (top).

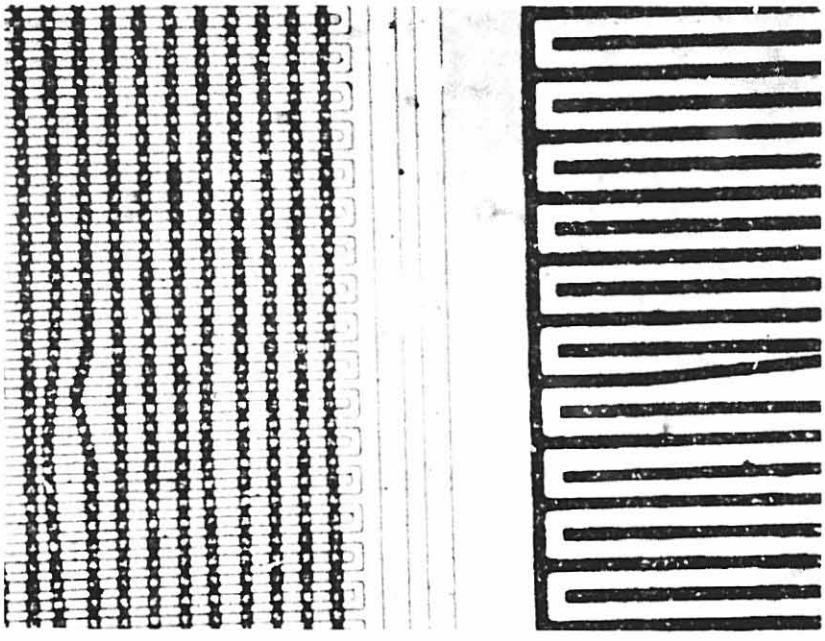


Figure 42. Wafer 7-15. 1μm PIQ plus doped plasma enhanced SiO_2. On this wafer, notice poor adhesion of second level metal to the oxide.

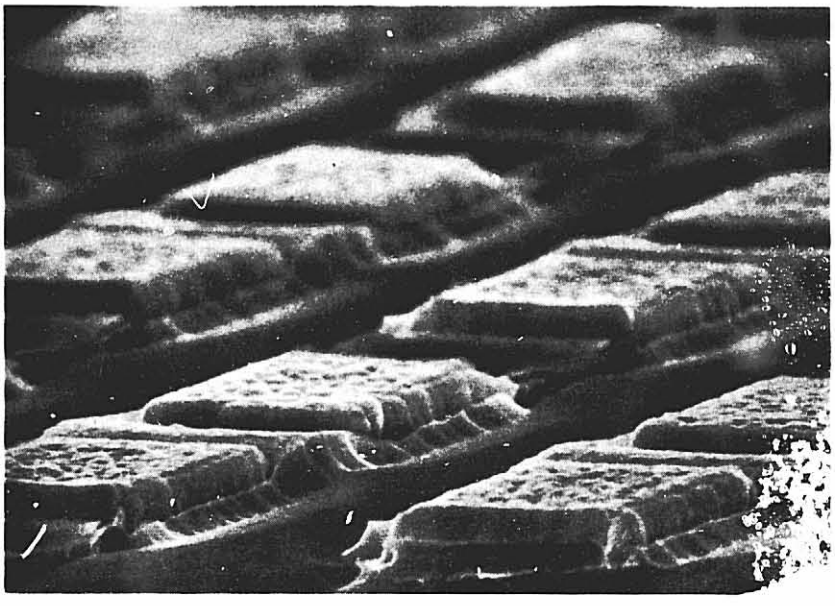


Figure 43. Via's of wafer 3-11, dielectric consisting of undoped plasma deposited SiO_2. Notice large via over-etch in processing these wafers. Magnification is 3300X.

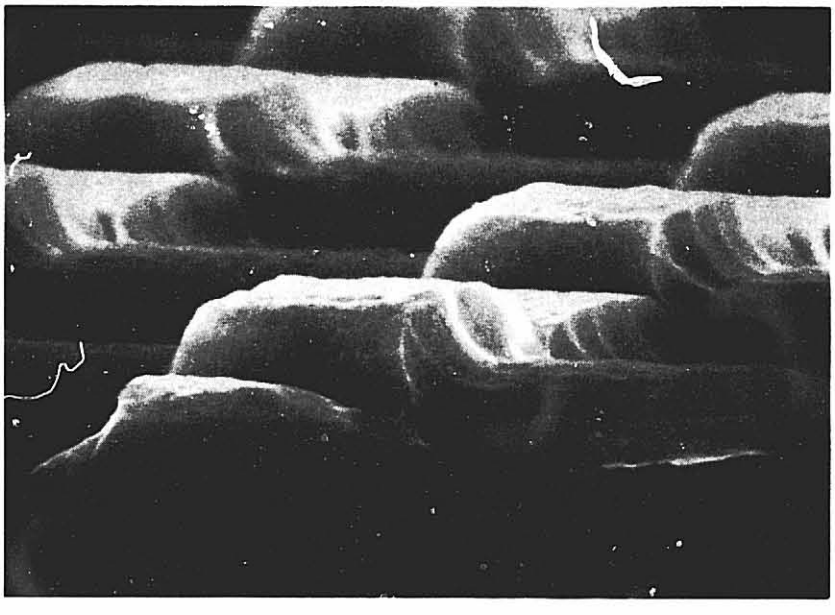


Figure 44. Cross-over of wafer 3-11. Notice excellent step coverage attainable with this dielectric. Magnification is 6050X.

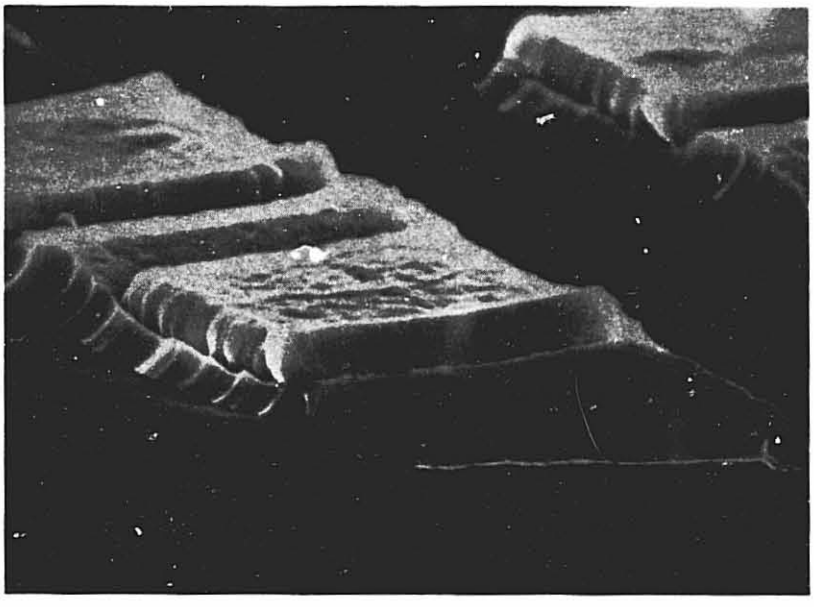


Figure 45. Via's of wafer 3-12, dielectric consist of phosphorous doped plasma deposited SiO_2. Notice over-etch of dielectric. Magnification is 4400X. (Processed by P.W. Corp.)

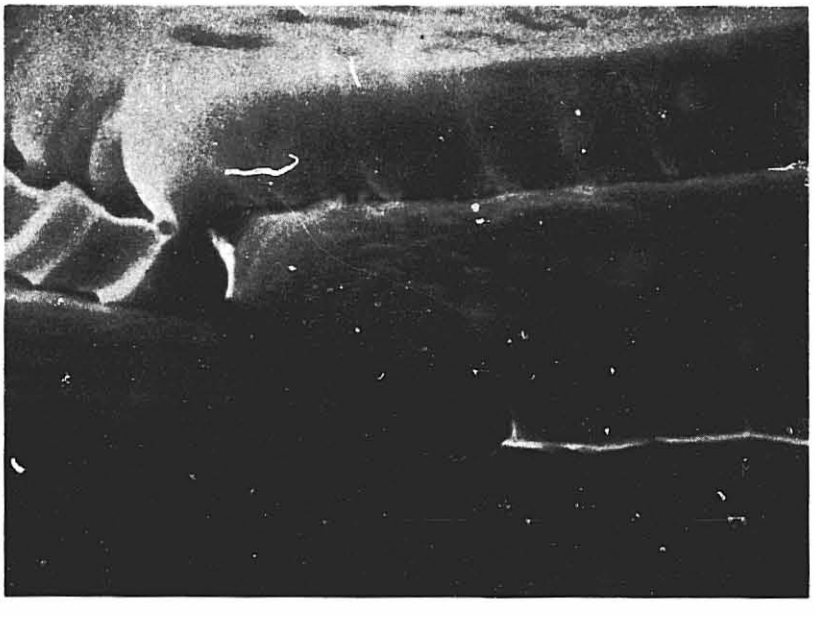


Figure 46. Magnification of above SEM micrograph illustrating dielectric and metal step-coverage. Magnification is 11,000X.

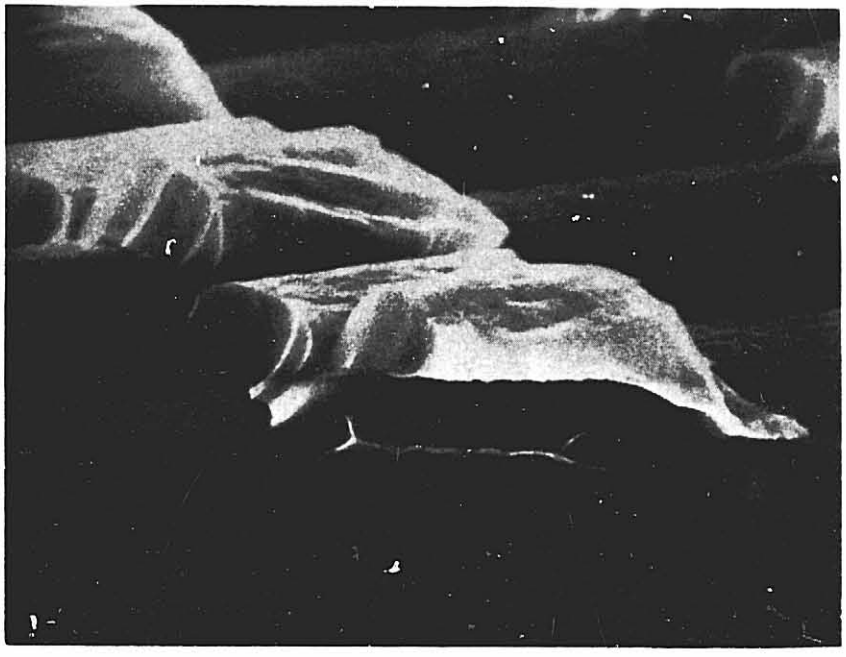


Figure 47. Cross-over of wafer 3-12. Magnification is 6600X.

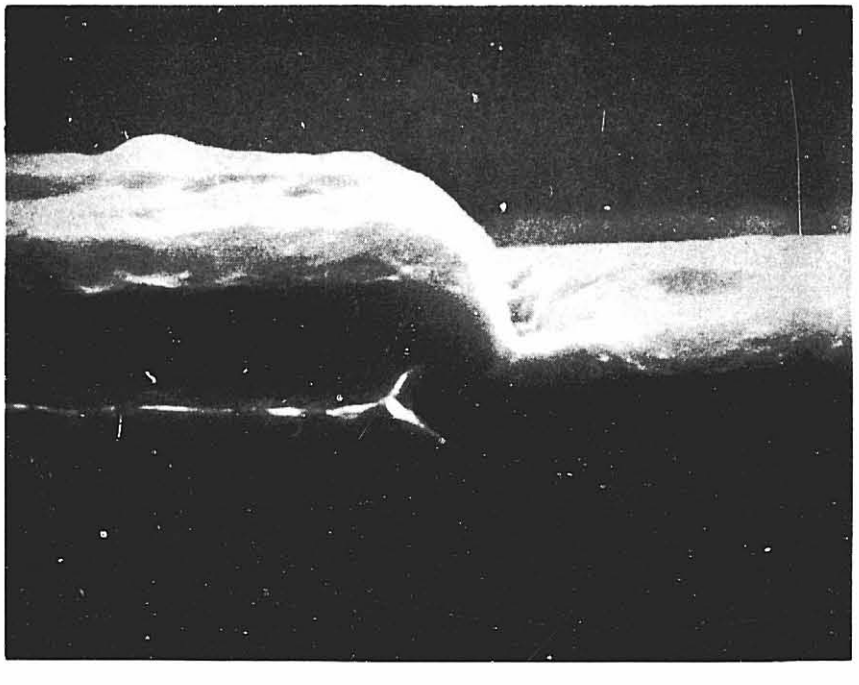


Figure 48. Cross-section of edge of big capacitor illustrating step coverage property of dielectric for wafer 3-12. Magnification is 11,000X.

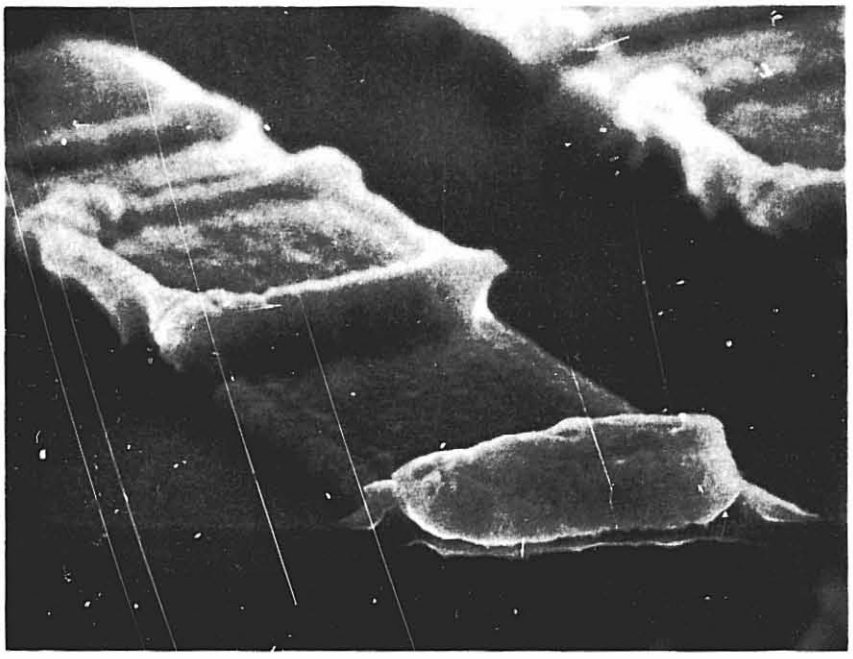


Figure 49. Via's of wafer 5-25, dielectric consist of approximately one micron undoped plasma deposited SiO_2. Magnification is 4400X.

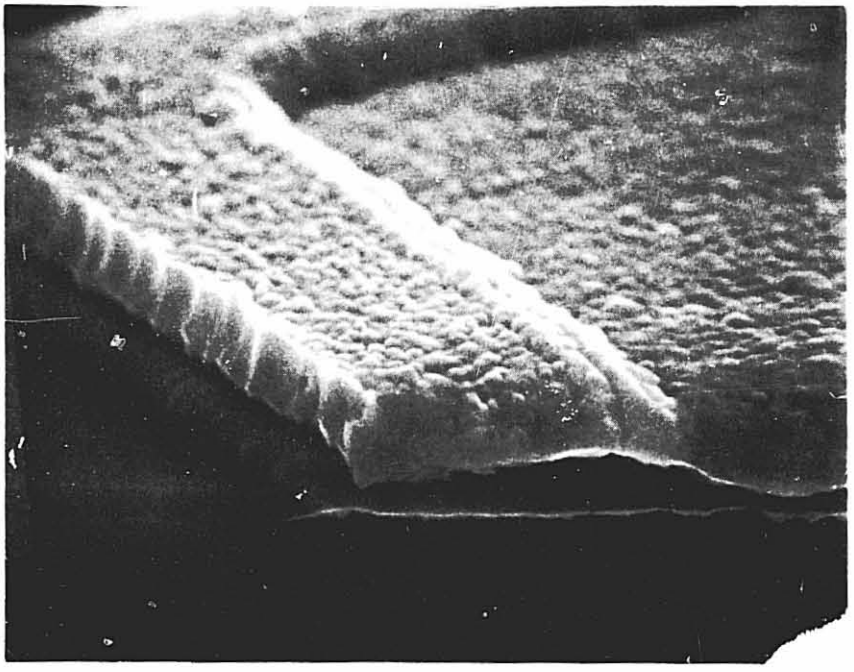


Figure 50. Cross-section of a via on wafer 5-25. Notice slight misalignment of metal. Magnification is 5500X.

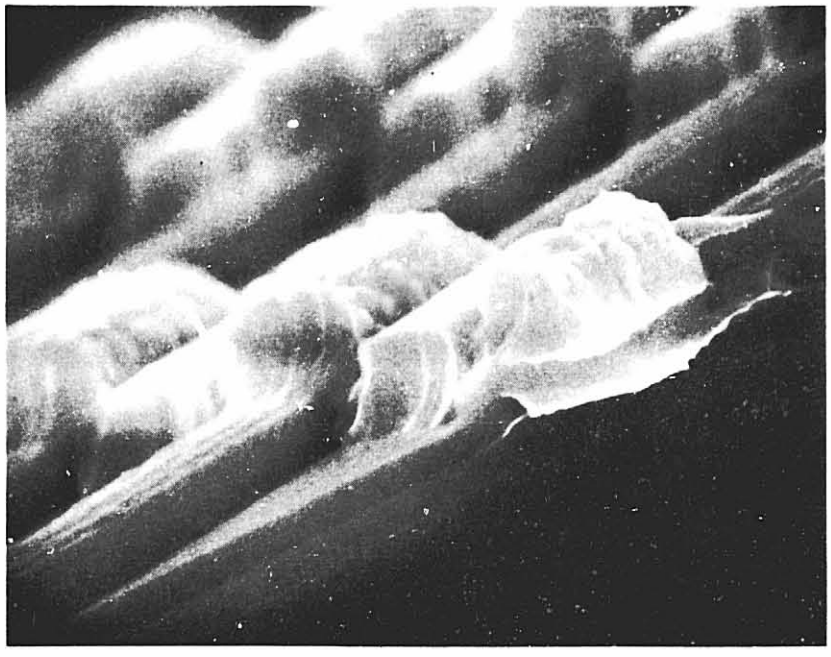


Figure 51. Cross-overs for wafer 5-25. Magnification is 6600X.

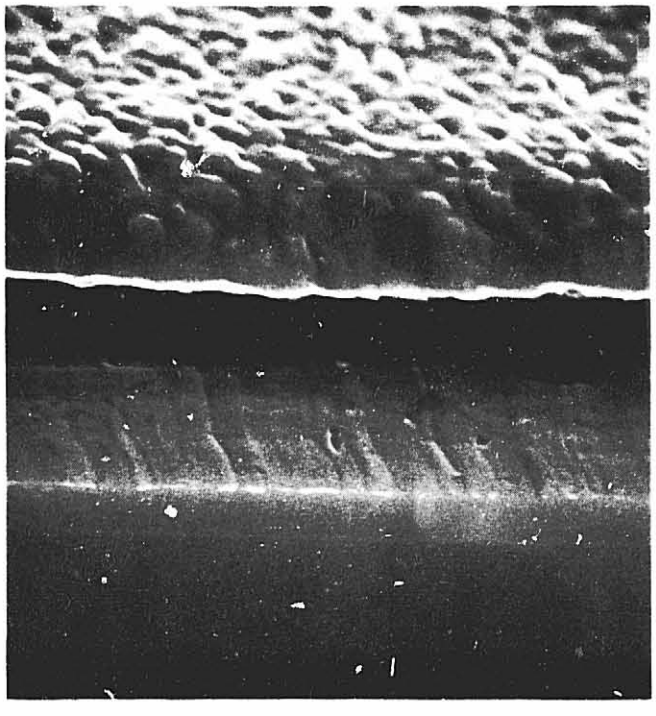


Figure 52. Cross-section of big capacitor for wafer 5-25 showing top layer Al/Si, plasma deposited SiO_2 (dark), bottom layer Al/Si and thermal oxide layer. Magnification is 8800X.

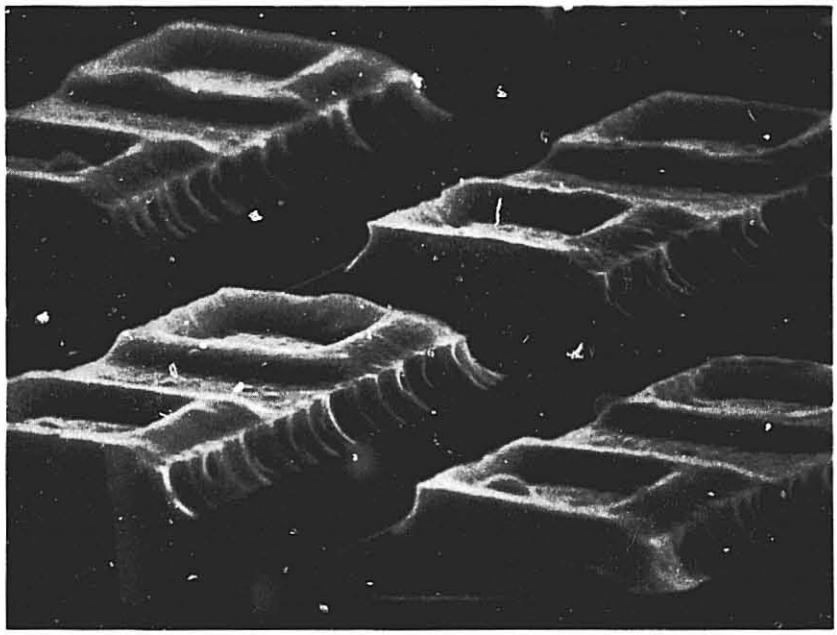


Figure 53. Via's of wafer 3-1, dielectric consist of polyimide PIQ-13 (top) and 0.25 μ phosphorous doped plasma deposited SiO_2 (bottom). Magnification is 3300X.

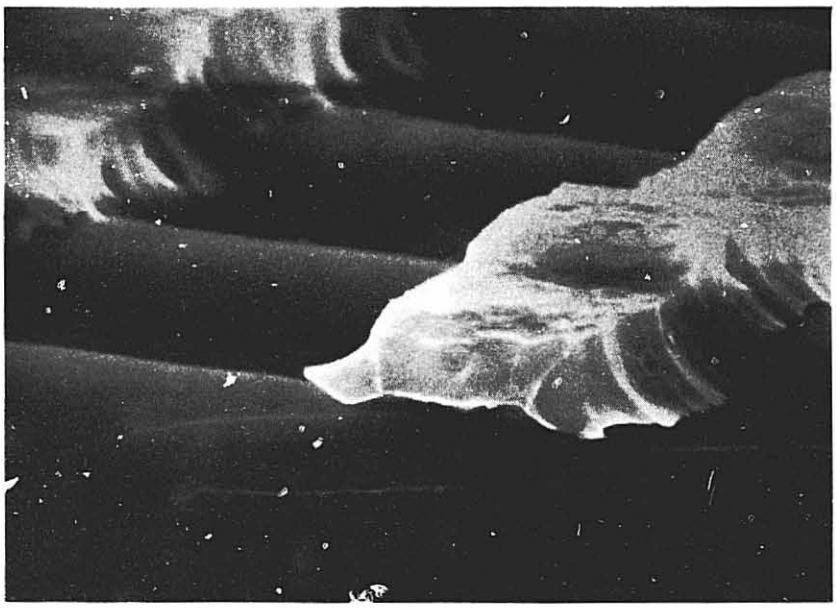


Figure 54. Cross-over of wafer 3-1. Notice planarization affect of polyimide. Magnification is 6600X.

WAFER NUMBER 5-14 DIELECTRIC TYPE UNDOPED SPUTTERED QUARTZ

CAPACITANCE (100KHZ) N/A pf DIELECTRIC THICKNESS .513microns

1st METAL(CO) RESISTANCE N/A ohms 2nd METAL(CO) RESISTANCE N/A ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	---	---	---	---	---	* - FINAL TEMPERATURE FOR
CROSS-OVER	---	---	---	---	---	POLYIMIDE IS 400'C
1st METAL(IF)	195	7350	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	115	16300	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.8	142.8				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	1	ALL	ALL	0	1
OPENS	0	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VIAS OVER ETCHED, PORTIONS OF THE CORNERS OF THE CAPACITOR SEEM TO BE MISSING, VERY POOR STEP COVERAGE, APPEARS TO HAVE RESIDUE ON TOP OF FIRST METAL, ALL CAPACITORS AND CROSS-OVERS SHORTED	NO APPARENT EFFECTS FROM THE ANNEALING, STILL RAGED LOOKING

Table 24. Summary of measured data and visual inspection for wafer 5-14.

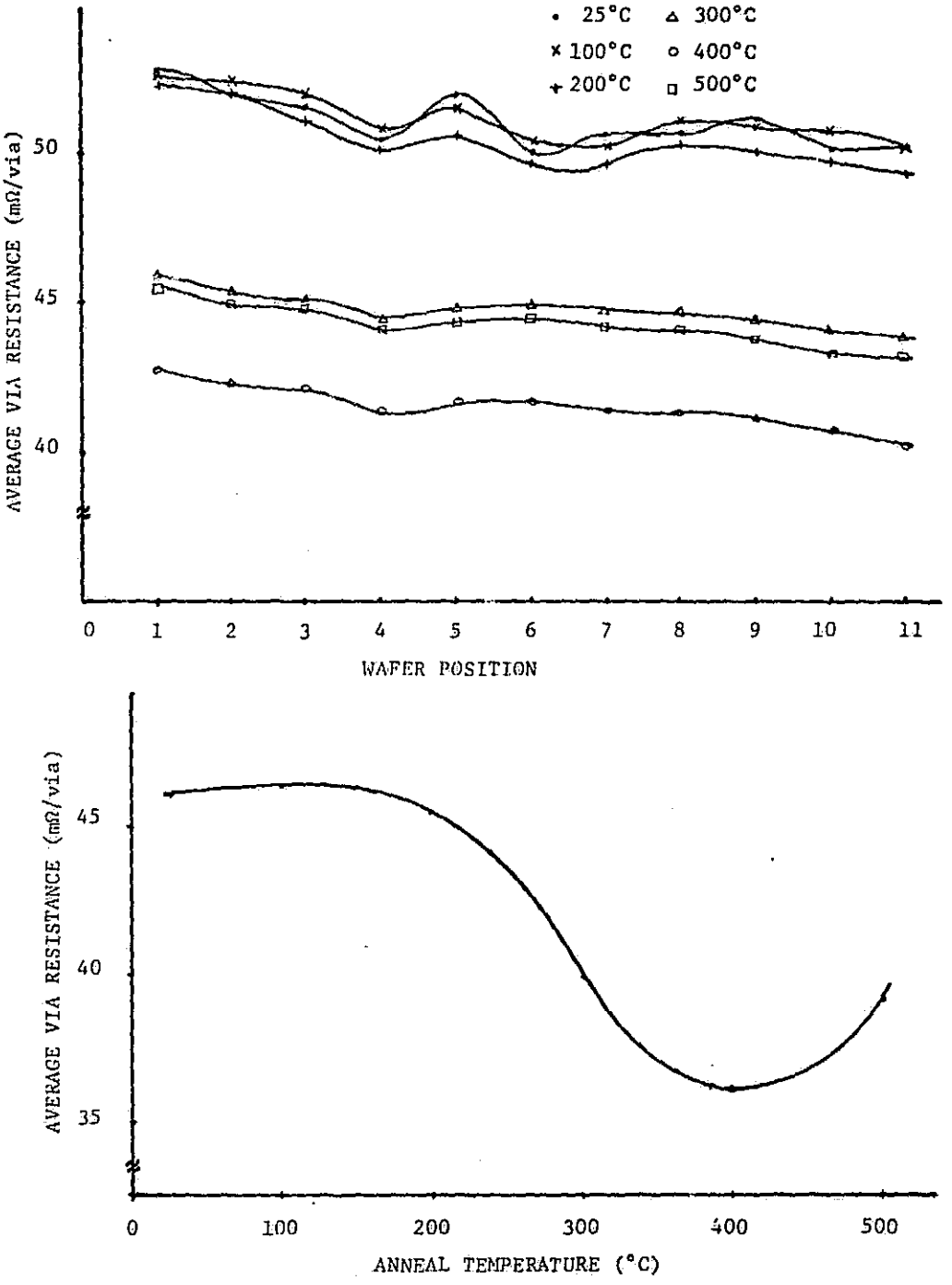


Figure 55. Wafer 5-14. The dielectric consist of 0.35 micron thick RF sputtered quartz.

WAFER NUMBER 5-21 DIELECTRIC TYPE UNDOPED SPUTTERED QUARTZ + PIQ

CAPACITANCE (100KHZ) 24pf DIELECTRIC THICKNESS 1microns

1st METAL(CO) RESISTANCE 1629ohms 2nd METAL(CO) RESISTANCE 280ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	3.2	2.2	260	230	220
CROSS-OVER	55	145	330	360	355
1st METAL(IF)	110	115	N/A	N/A	N/A
2nd METAL(IF)	80	140	N/A	N/A	N/A
MEASURING VOLTAGE	71.4	71.4			

* FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R>10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	1	1	1	2	2	0	1
OPENS	2	0	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, NO SIGN OF LIFTING	BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 25. Summary of measured data and visual inspection for wafer 5-21.

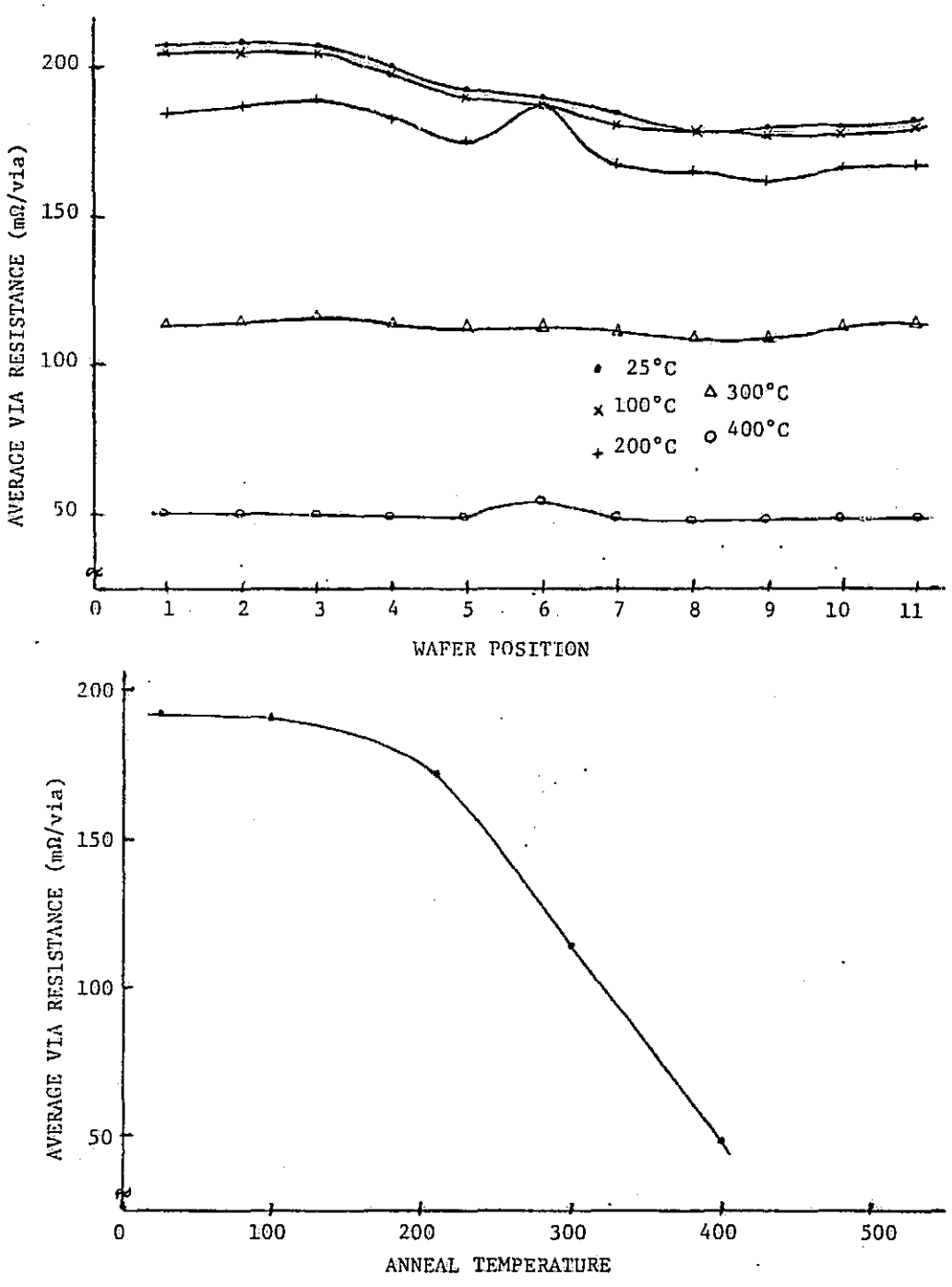


Figure 56. Wafer 5-21. The dielectric consist of 0.11 microns of RF sputtered quartz (bottom) plus 0.9 microns of Hitachi PIQ-13 polyimide (top).

WAFER NUMBER 8-3 DIELECTRIC TYPE PIQ + UNDOPED SPUTTERED QUARTZ

CAPACITANCE (100KHZ) 37.625pf DIELECTRIC THICKNESS .7microns

1st METAL(CO) RESISTANCE 159ohms 2nd METAL(CO) RESISTANCE 319ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	28.7	7.5	230	180	180
CROSS-OVER	240	145	135	100	135
1st METAL(IF)	35	80	N/A	N/A	N/A
2nd METAL(IF)	70	120	N/A	N/A	N/A
MEASURING VOLTAGE	71.4	71.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1040	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	3	2	0	2
OPENS	1	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
ENTIRE PORTIONS OF QUARTZ MISSING, SOME QUARTZ MISSING BETWEEN THE CAPACITOR PLATES, GOOD STEP COVERAGE DUE TO THE PIQ	BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 26. Summary of measured data and visual inspection for wafer 8-3.

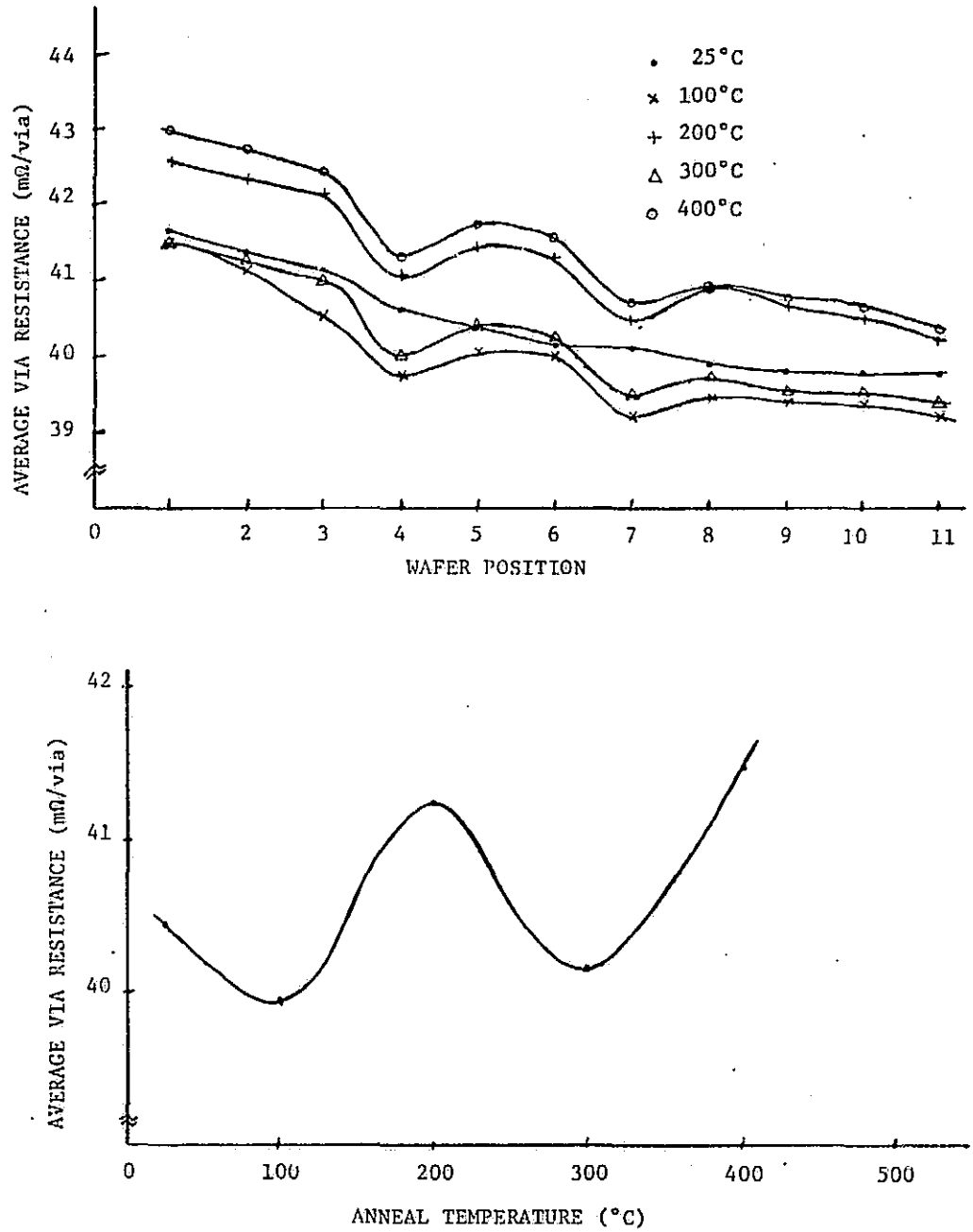


Figure 57. Wafer 8-3. The dielectric consist of 0.6 microns of Hitachi PIQ-13 (bottom) plus 0.11 microns of RF sputtered quartz (top).

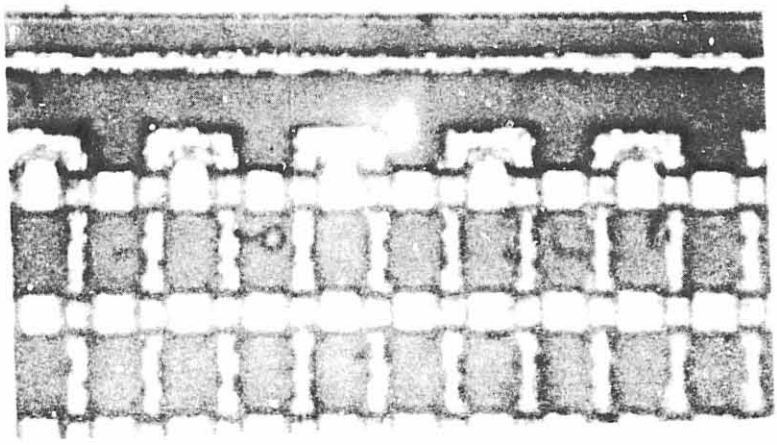


Figure 58. Wafer 5-14. 0.5μm sputtered quartz The quartz is left on top of the first level metal only in the center, outter edges are bare.

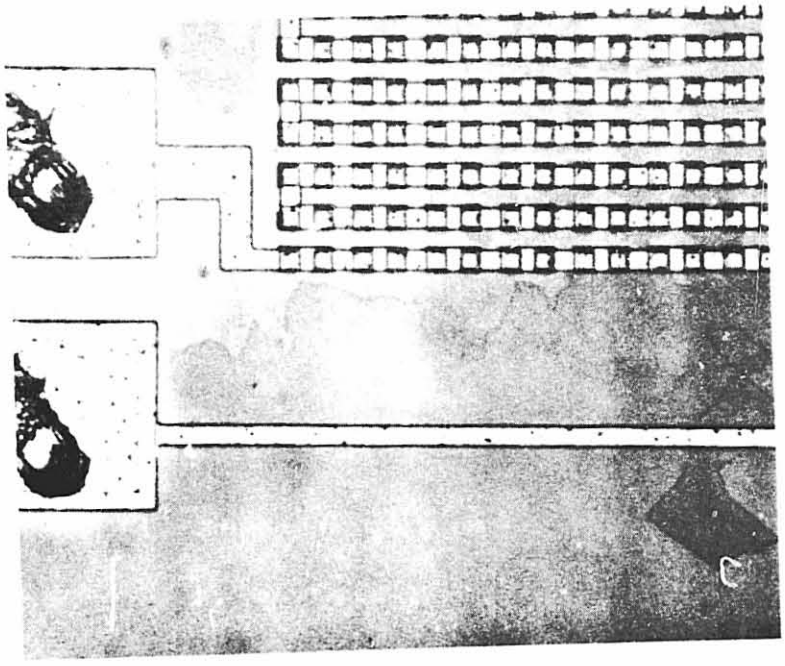


Figure 59. Wafer 8-3. PIQ plus sputtered quartz on top. Notice in areas that entire portions of quartz is missing (believed to be removed in processing).

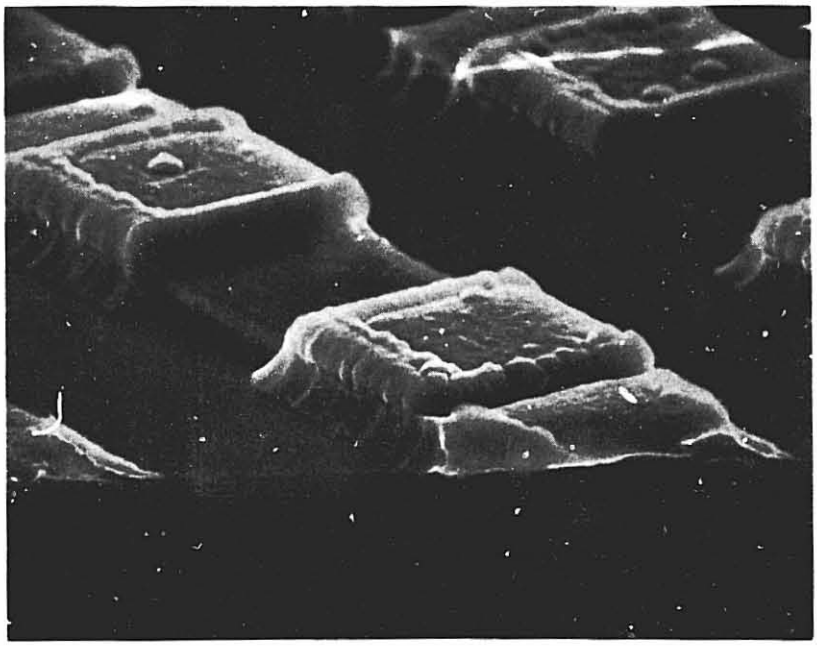


Figure 60. Via's of wafer 5-15, dielectric consist of sputtered quartz. Magnification is 3300X.

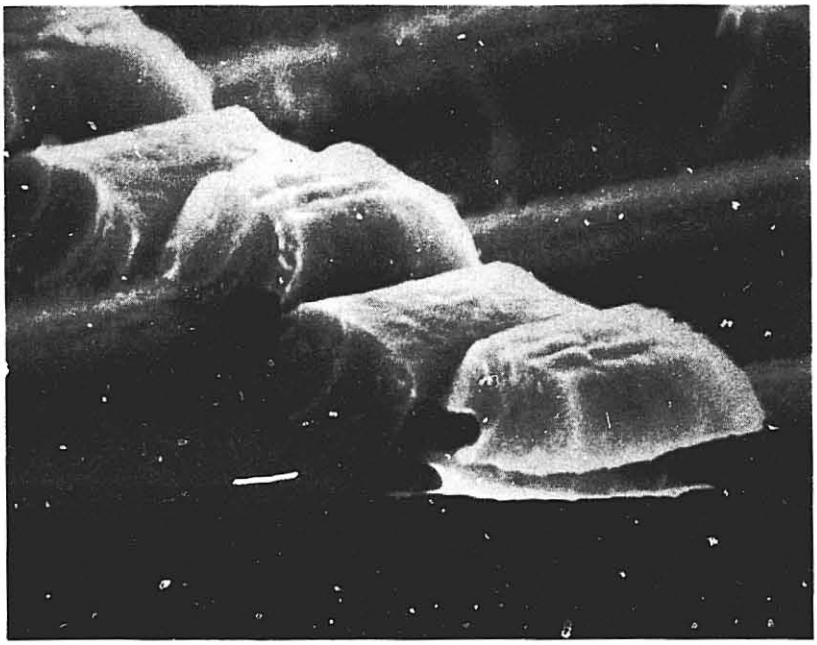


Figure 61. Cross-over of wafer 5-15. Notice "mouse-holes" at steps. Magnification is 6600X.

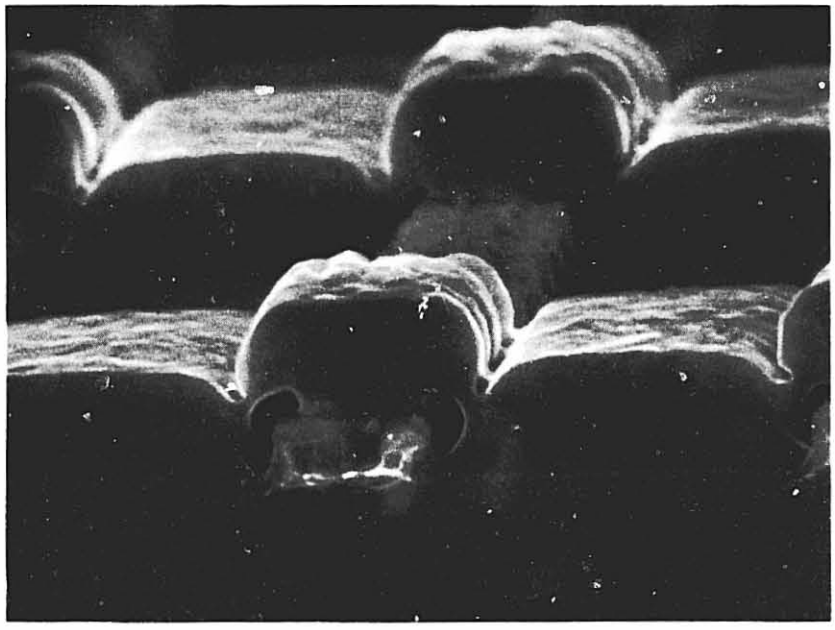


Figure 62. Perpendicular view of cross-overs of wafer 5-15 illustrating step-coverage problems. Magnification is 6600X.

Figure 63. Cross-section of big capacitor for wafer 5-15 showing thickness of top layer Al/Si, quartz dielectric, and bottom layer Al/Si. Magnification is 8800X.

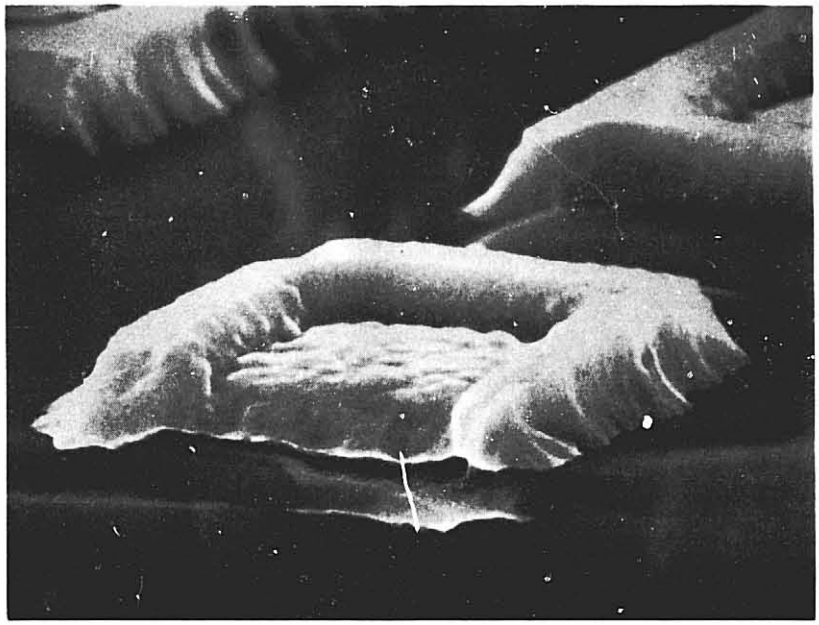


Figure 64. Via of wafer 5-20, dielectric consist of 0.11 μ quartz (bottom) and approximately 1 μ polyimide PIQ-13 (top). Magnification is 5500X.

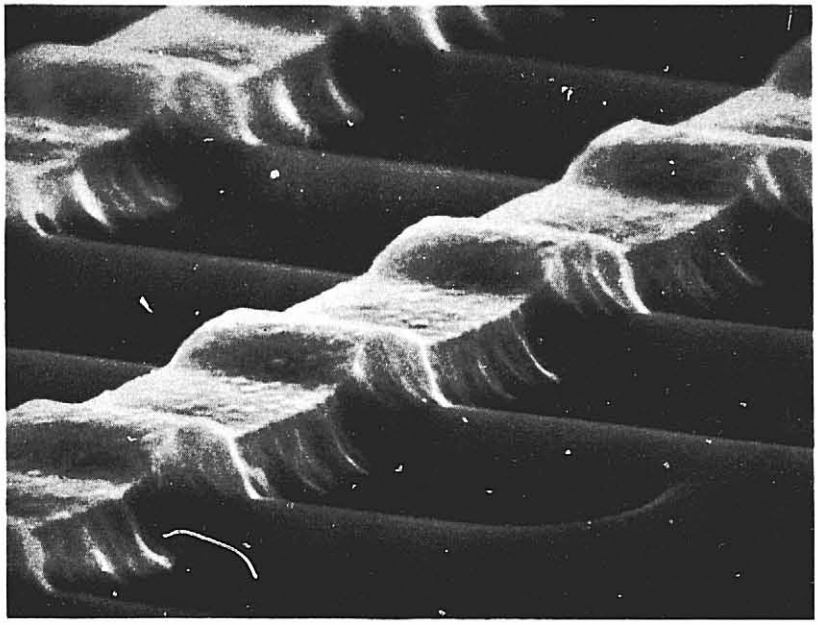


Figure 65. Cross-over of wafer 5-20. Notice planarization of dielectric. Magnification is 5500X.

WAFER NUMBER 5-3 DIELECTRIC TYPE PLASMA NITRIDE

CAPACITANCE (100KHZ) 47.125pf DIELECTRIC THICKNESS 1microns

1st METAL(CO) RESISTANCE 1721ohms 2nd METAL(CO) RESISTANCE 473ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	7	12.2	520	510	450
CROSS-OVER	3400	1700	400	460	365
1st METAL(IF)	635	200	N/A	N/A	N/A
2nd METAL(IF)	560	315	N/A	N/A	N/A
MEASURING VOLTAGE	142.8	142.8			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	11	20	0	1
OPENS	0	1	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
POOR SHAPED VIAS, SOME UNDER ETCHED AND SOME OVER ETCHED, STEEP STEPS, RAGED LOOKING	NO BUBBLING, BREAKDOWNS OCCURRED AT STEPS

Table 27. Summary of measured data and visual inspection for wafer 5-3.

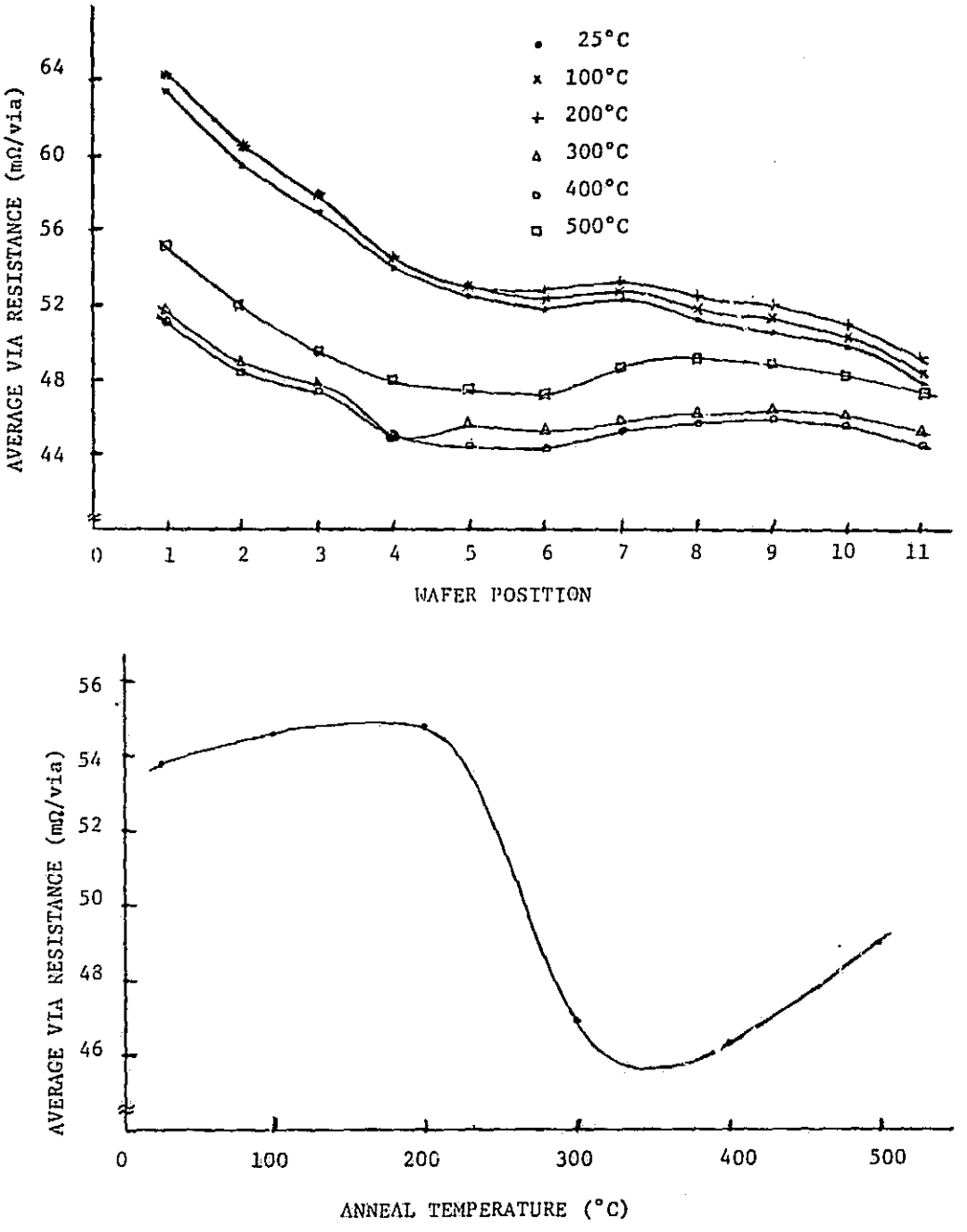


Figure 66. Wafer 5-3. The dielectric consist of 1.0 microns of plasma enhanced nitride.

WAFER NUMBER 5-12 DIELECTRIC TYPE PLASMA NITRIDE + PIQ

CAPACITANCE (100KHZ) 21pf DIELECTRIC THICKNESS 1.05microns

1st METAL(CO) RESISTANCE 1475ohms 2nd METAL(CO) RESISTANCE 318ohms

	LEAKAGE CURRENT(pa)		BREBREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	34.3	.5	590	600	525	*- FINAL TEMPERATURE FOR
CROSS-OVER	440	455	525	545	400	POLYIMIDE IS 400'C
1st METAL(IF)	130	250	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	230	365	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	214.4	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	0	1
OPENS	0	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VISIBLE DIFERENCE IN THE ETCHING OF THE TWO LAYERS, GOOD STEP COVERAGE	BUBBLING IN THE CENTER DIE, SOME BREAKDOWNS OCCURRED BETWEEN THE PADS, SOME SIGNS OF LIFTING AROUND THE EDGES OF THE WAFER

Table 28. Summary of measured data and visual inspection for wafer 5-12.

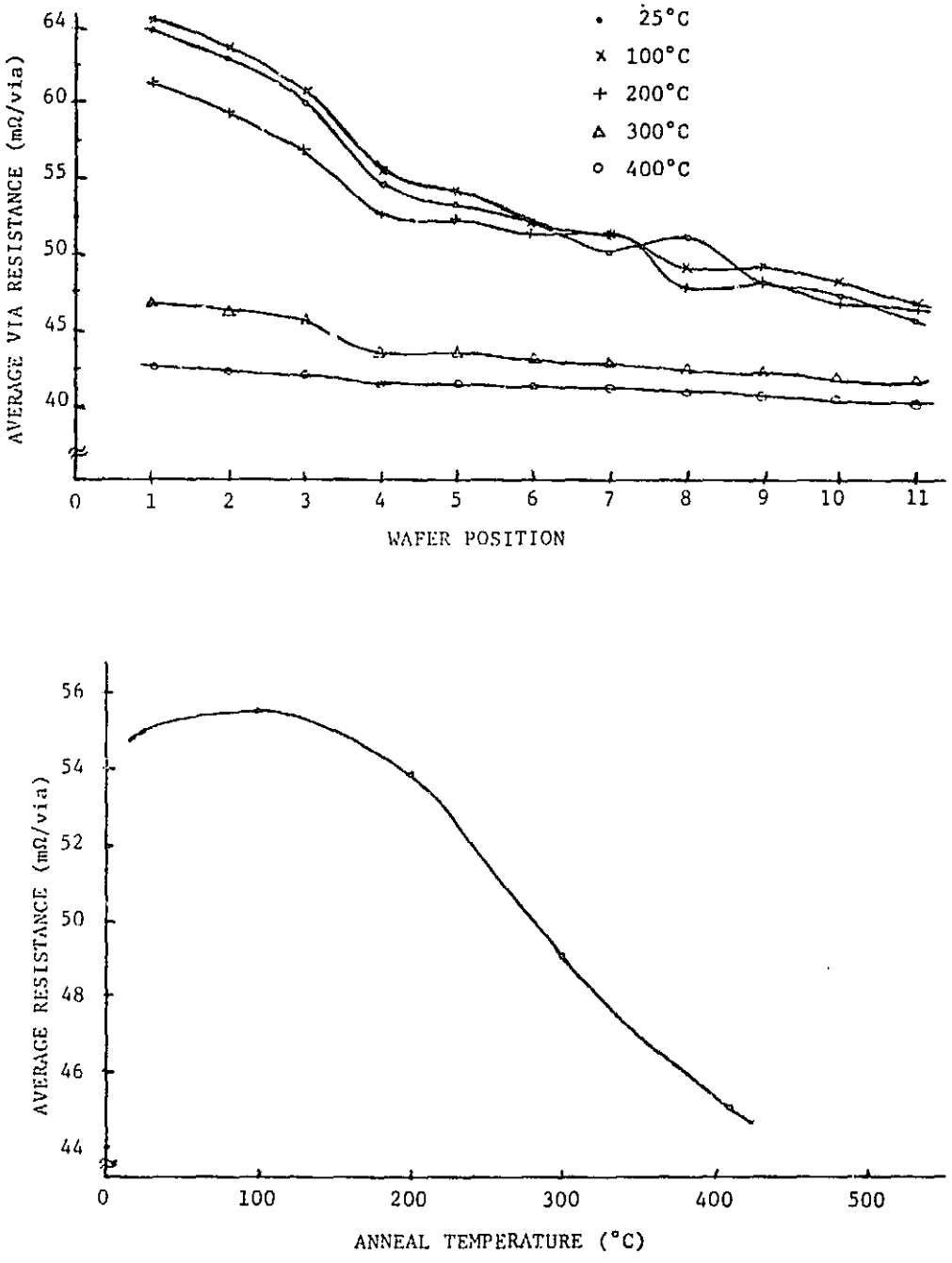


Figure 67. Wafer 5-12. The dielectric consist of 0.25 microns of plasma enhanced nitride (bottom) plus 0.85 microns of Hitachi PIQ-13 (top).

C-2

WAFER NUMBER	8-10		DIELECTRIC TYPE PIQ + PLASMA NITRIDE			
CAPACITANCE (100KHZ)	32.125pf		DIELECTRIC THICKNESS			.71microns
1st METAL(CO) RESISTANCE	1171ohms		2nd METAL(CO) RESISTANCE			305ohms
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	70.3	.6	410	405	400	*- FINAL TEMPERATURE FOR
CROSS-OVER	740	240	310	290	270	POLYIMIDE IS 400'C OTHERS 500'C
1st METAL(IF)	60	135	N/A	N/A	N/A	(CO)- CROSS-OVER (IF)- INTERDIGITATED
2nd METAL(IF)	100	220	N/A	N/A	N/A	FINGERS (NO)- NORMALLY OPEN
MEASURING VOLTAGE	142.8	142.8				OPEN- R)10Megohm

VIA CHAINS					INTERDIGITATED FINGERS	
1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	1	0	0	1	0	1
OPENS	1	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
EXCELLENT VIA DEFINITION, GOOD STEP COVERAGE, NO SIGN OF LIFTING	NO BUBBLING, NO SIGN OF LIFTING, LOOK VERY GOOD

Table 29. Summary of measured data and visual inspection for wafer 8-10.

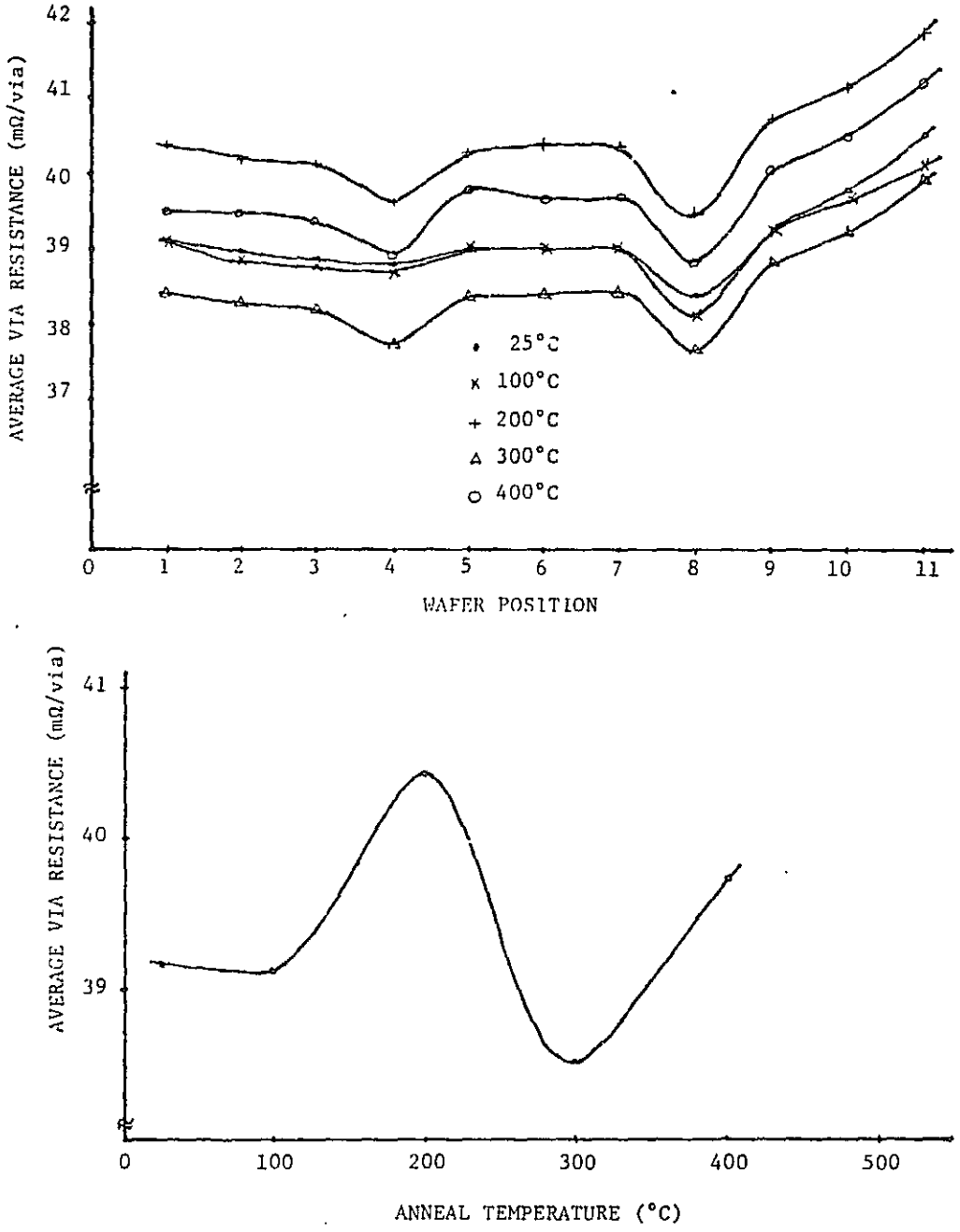


Figure 68. Wafer 8-10. The dielectric consist of 0.45 microns Hitachi PIQ-13 (bottom) plus 0.25 microns plasma enhanced nitride (top).

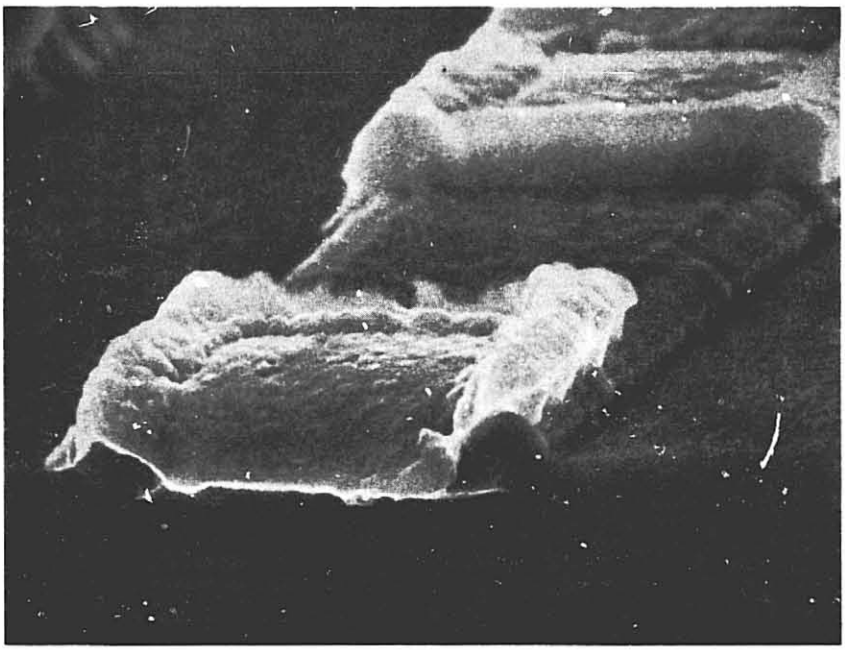


Figure 69. Cross-section of via for wafer 5-2, dielectric consist of plasma deposited silicon nitride. Magnification is 5500X.

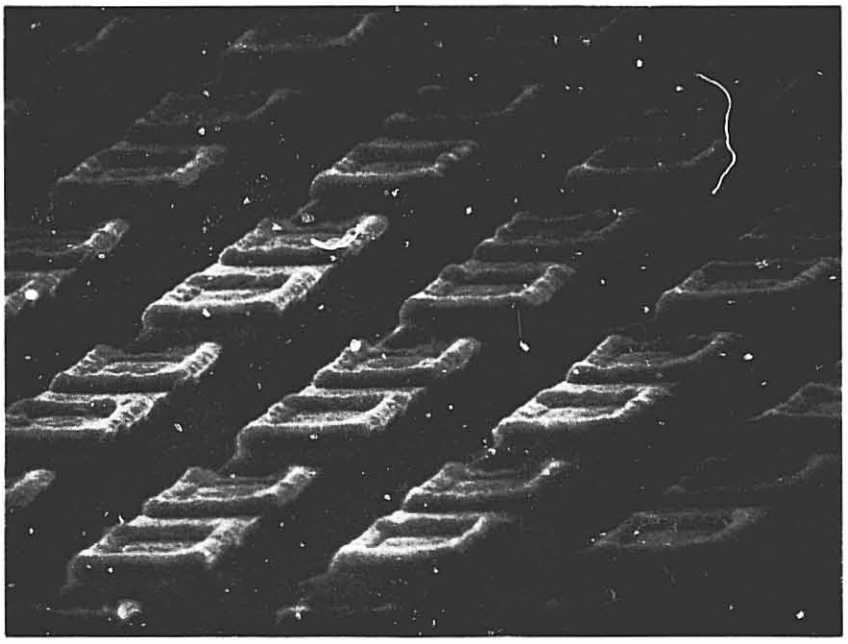


Figure 70. Via section of wafer 5-2 illustrating incomplete removal of photoresist layer. Magnification is 1650X.

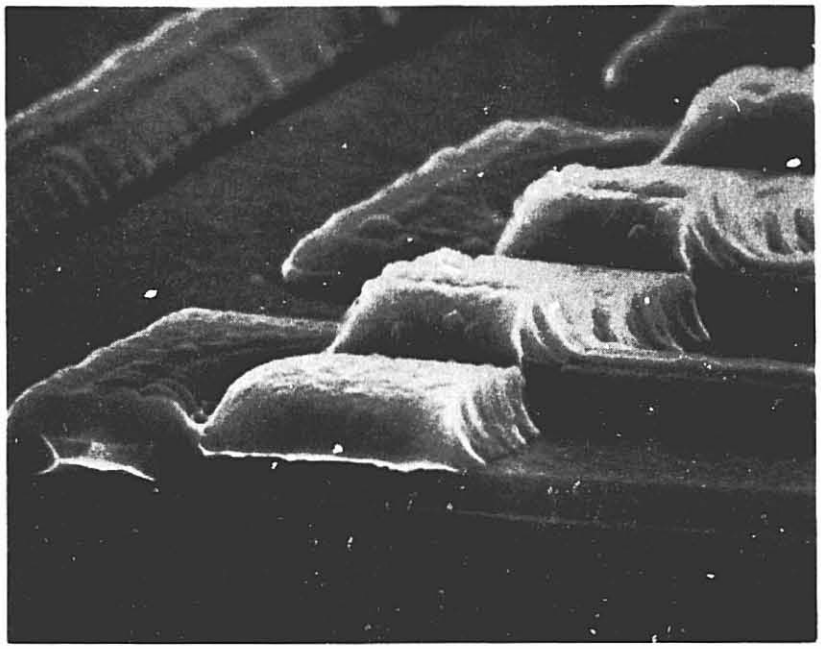


Figure 71. Cross-over of wafer 5-2 illustrating step-coverage dielectric. Magnification is 5500X.

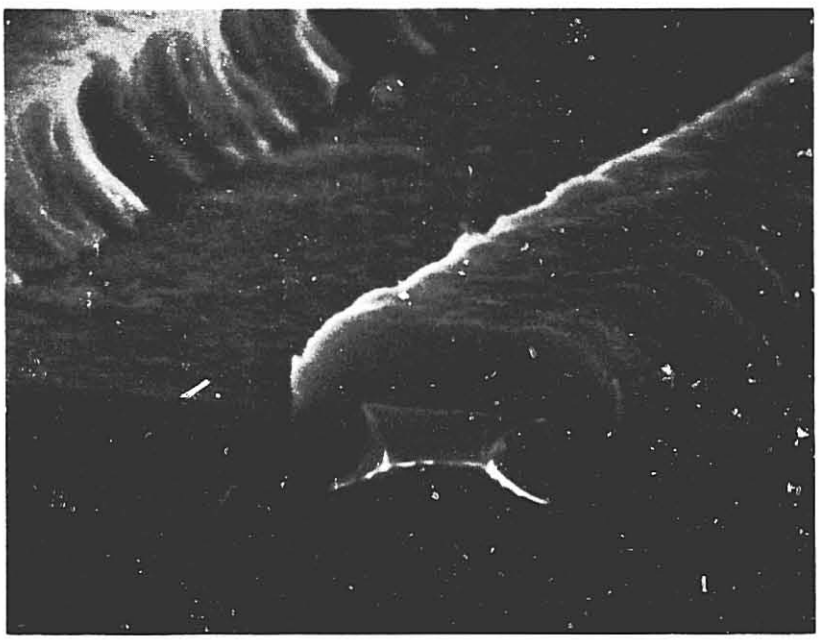


Figure 72. Magnification of a first layer metal interconnect covered with dielectric for wafer 5-2. Notice the excellent step-coverage and slight 'cusping' of dielectric. Magnification is 11,000X.

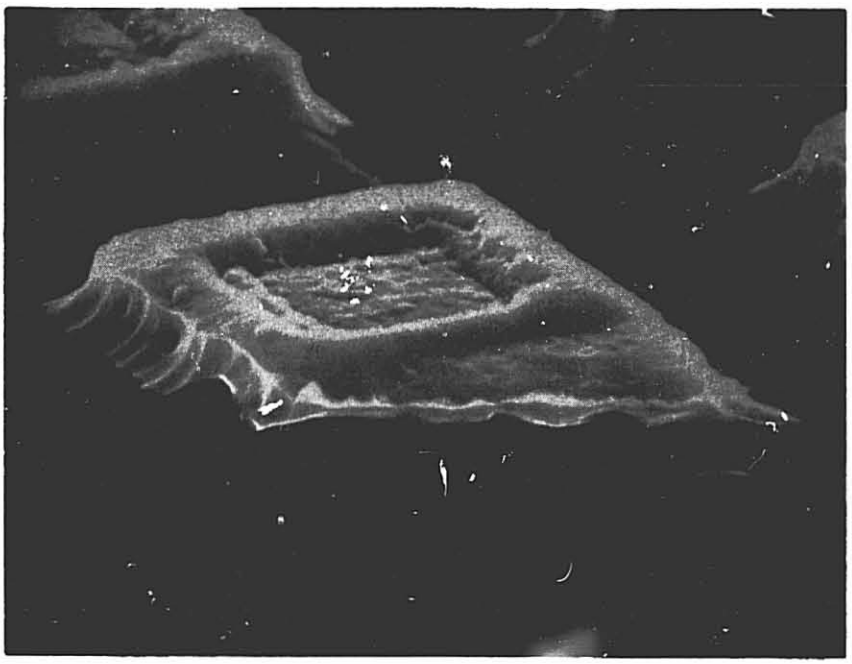


Figure 73. Via of wafer 7-19, dielectric consist of approximately 0.75 μ polyimide PI-2555 (bottom) and 0.25 μ plasma deposited silicon nitride (top). Magnification is 4400X.

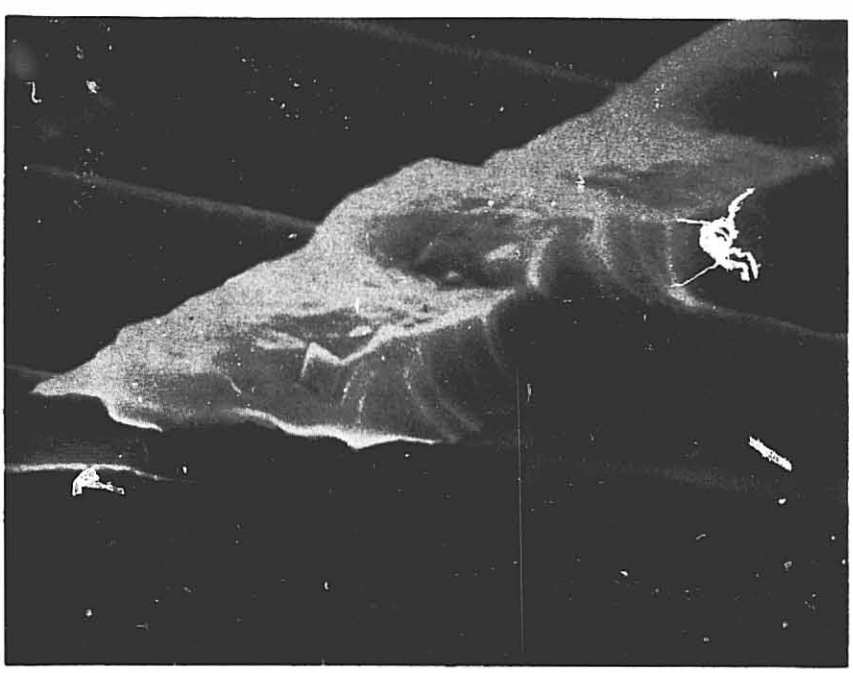


Figure 74. Cross-over of wafer 7-19. Magnification is 6600X.

WAFER NUMBER 9-16 DIELECTRIC TYPE 2555

CAPACITANCE (100KHZ) 22pf DIELECTRIC THICKNESS .6microns

1st METAL(CO) RESISTANCE 2730ohms 2nd METAL(CO) RESISTANCE 203ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	10.7	.2	475	430	310
CROSS-OVER	170	205	390	350	350
1st METAL(IF)	95	165	N/A	N/A	N/A
2nd METAL(IF)	145	240	N/A	N/A	N/A
MEASURING VOLTAGE	142.8	142.8			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	0	1
OPENS	0	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
EXCELLENT VIA DEFINITION, NO SIGNS OF LIFTING	BUBBLING IN THE CENTER DIE, NO SIGNS OF LIFTING

Table 30. Summary of measured data and visual inspection for wafer 9-16.

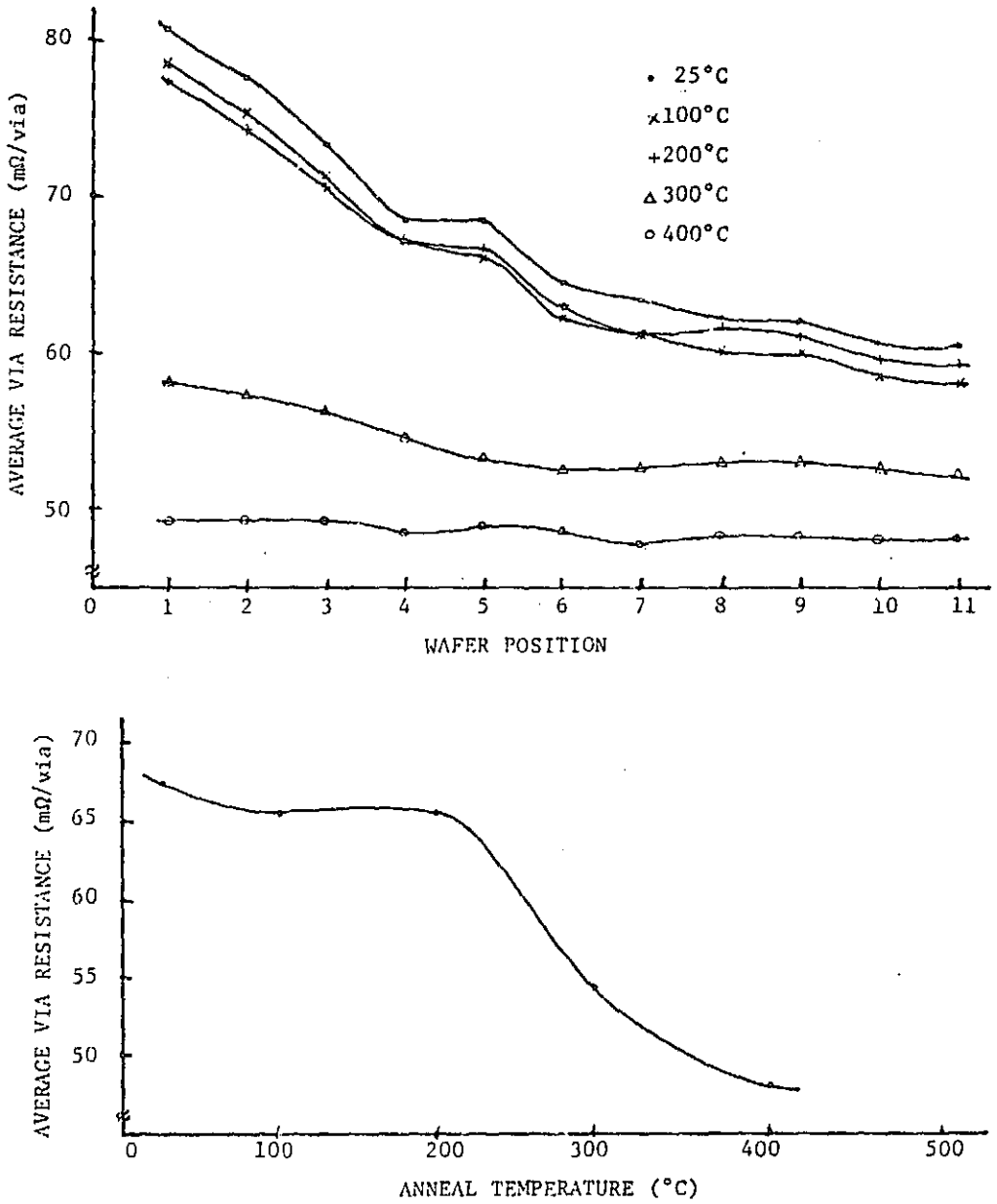


Figure 75. Wafer 9-16. The dielectric consist of 1.0 microns of Dupont PI-2555.

WAFER NUMBER	9-25		DIELECTRIC TYPE		PIQ	
CAPACITANCE (100KHZ)	30.3pf		DIELECTRIC THICKNESS		.89microns	
1st METAL(CO) RESISTANCE	1047ohms		2nd METAL(CO) RESISTANCE		305ohms	
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	3.1	4.9	260	245	200	*- FINAL TEMPERATURE FOR
CROSS-OVER	55	155	290	275	190	POLYIMIDE IS 400'C
1st METAL(IF)	35	90	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	65	135	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	71.4	71.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	1	1	0	0	1
OPENS	1	1	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, GOOD ADHERANCE, GOOD STEP COVERAGE	BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 31. Summary of measured data and visual inspection for wafer 9-25.

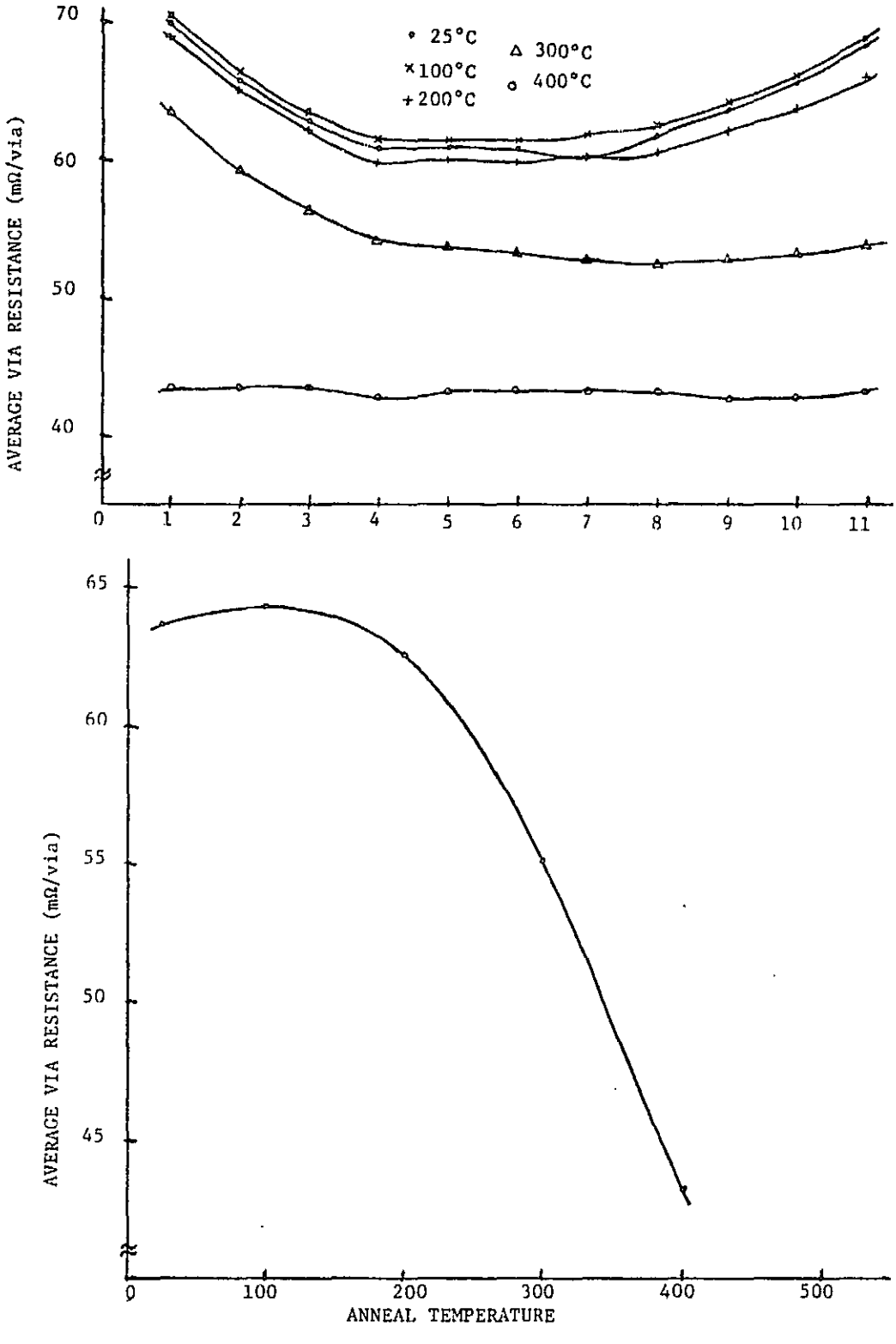


Figure 76. Wafer 9-25. The dielectric consist of 0.8 microns of Hitachi PIQ-13.

WAFER NUMBER 8-18 DIELECTRIC TYPE 2555

CAPACITANCE (100KHZ) 15pf DIELECTRIC THICKNESS 1microns

1st METAL(CO) RESISTANCE 1330ohms 2nd METAL(CO) RESISTANCE 266ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	.05	.2	620	555	565
CROSS-OVER	410	560	635	510	515
1st METAL(IF)	330	315	N/A	N/A	N/A
2nd METAL(IF)	410	500	N/A	N/A	N/A
MEASURING VOLTAGE	200	214.4			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R>10Megohm

VIA CHAINS			INTERDIGITATED FINGERS			
1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS 0	0	0	0	1	1	1
OPENS 0	12	13	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
SLIGHTLY ROUNDED VIAS, GOOD SLOPE ON SIDEWALLS OF VIAS, GOOD STEP COVERAGE, NO SIGN OF 2nd METAL LIFT-OFF	SOME BREAKDOWNS OCCURED BETWEEN PADS, BUBBLING IN CENTER DIE, NO SIGNS OF LIFT-OFF

Table 32. Summary of measured data and visual inspection for wafer 8-18.

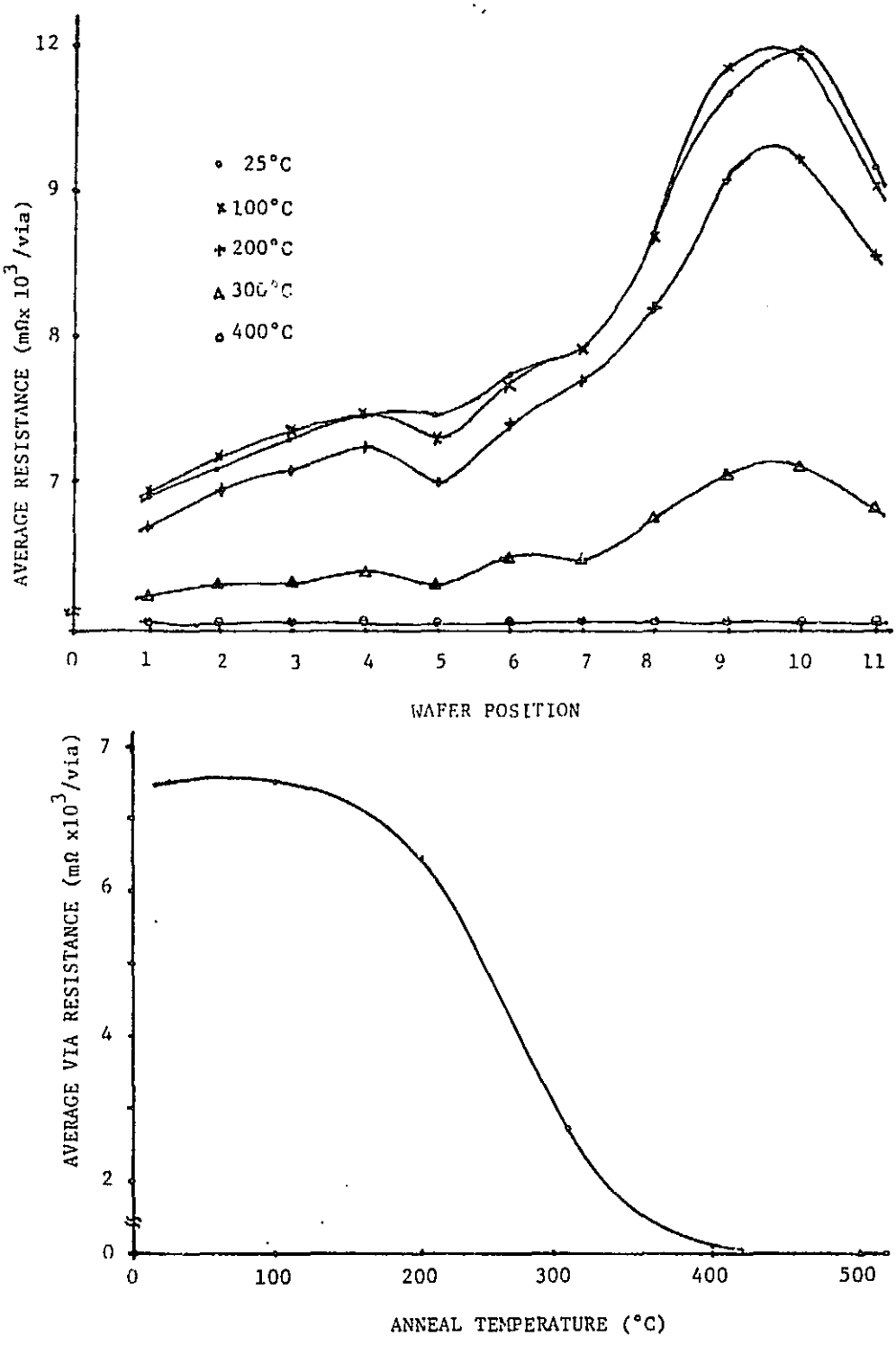


Figure 77. Wafer 8-18. The dielectric consist of 1.5 microns thick Dupont polyimide PI-2555.

WAFER NUMBER	8-20	DIELECTRIC TYPE	2545
CAPACITANCE (100KHZ)	32pf	DIELECTRIC THICKNESS	1.1microns
1st METAL(CO) RESISTANCE	1048ohms	2nd METAL(CO) RESISTANCE	310ohms

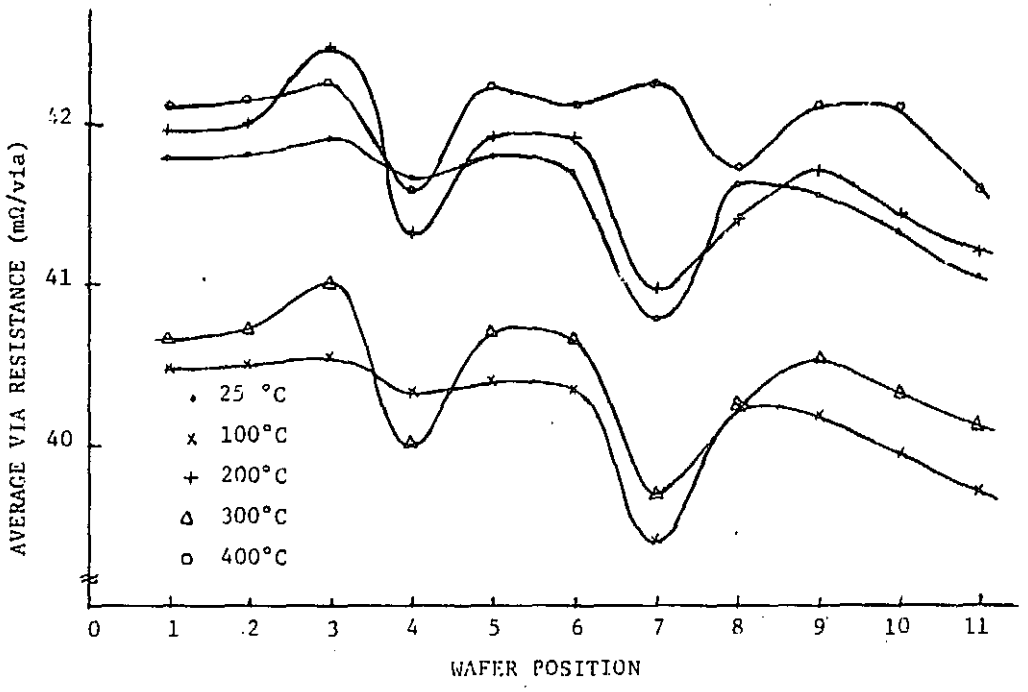
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	52.1	1	320	310	320	*- FINAL TEMPERATURE FOR
CROSS-OVER	245	290	300	310	310	POLYIMIDE IS 400'C
1st METAL(IF)	115	160	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	215	235	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.0	142.0				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R>10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1080	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	1	2
OPENS	2	1	4	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, GOOD STEP COVERAGE	NO BUBBLING, NO SIGN OF LIFTING

Table 33. Summary of measured data and visual inspection for wafer 8-20.



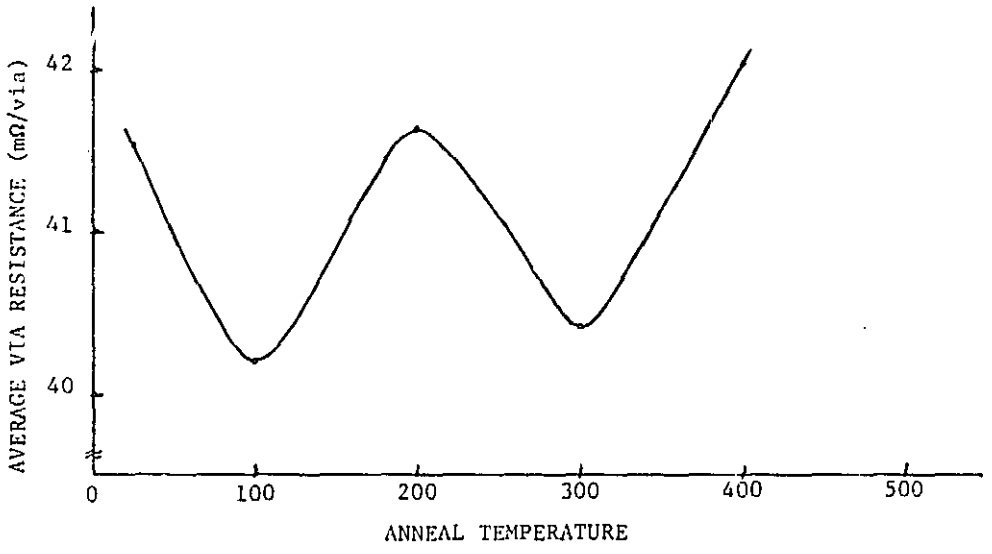


Figure 78. Wafer 8-20. The dielectric consist of 1.1 microns of Dupont PI-2545 polyimide.

WAFER NUMBER	8-22		DIELECTRIC TYPE		PIQ	
CAPACITANCE (100KHZ)		22pf	DIELECTRIC THICKNESS		1.475microns	
1st METAL(CO) RESISTANCE		991ohms	2nd METAL(CO) RESISTANCE		285ohms	
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	35 'C	FINAL *	35 'C	200 'C	FINAL *	
CAPACITOR	7.1	.05	405	495	470	*- FINAL TEMPERATURE FOR
CROSS-OVER	135	275	480	480	470	POLYIMIDE IS 400'C
1st METAL(IF)	75	155	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	130	230	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	142.8	142.8				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

VIA CHAINS					INTERDIGITATED FINGERS	
1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS 0	0	0	0	0	0	1
OPENS 1	0	0	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, GOOD STEP COVERAGE	BUBBLING IN THE CENTER DIE, NO SIGN OF LIFTING

Table 34. Summary of measured data and visual inspection for wafer 8-22.

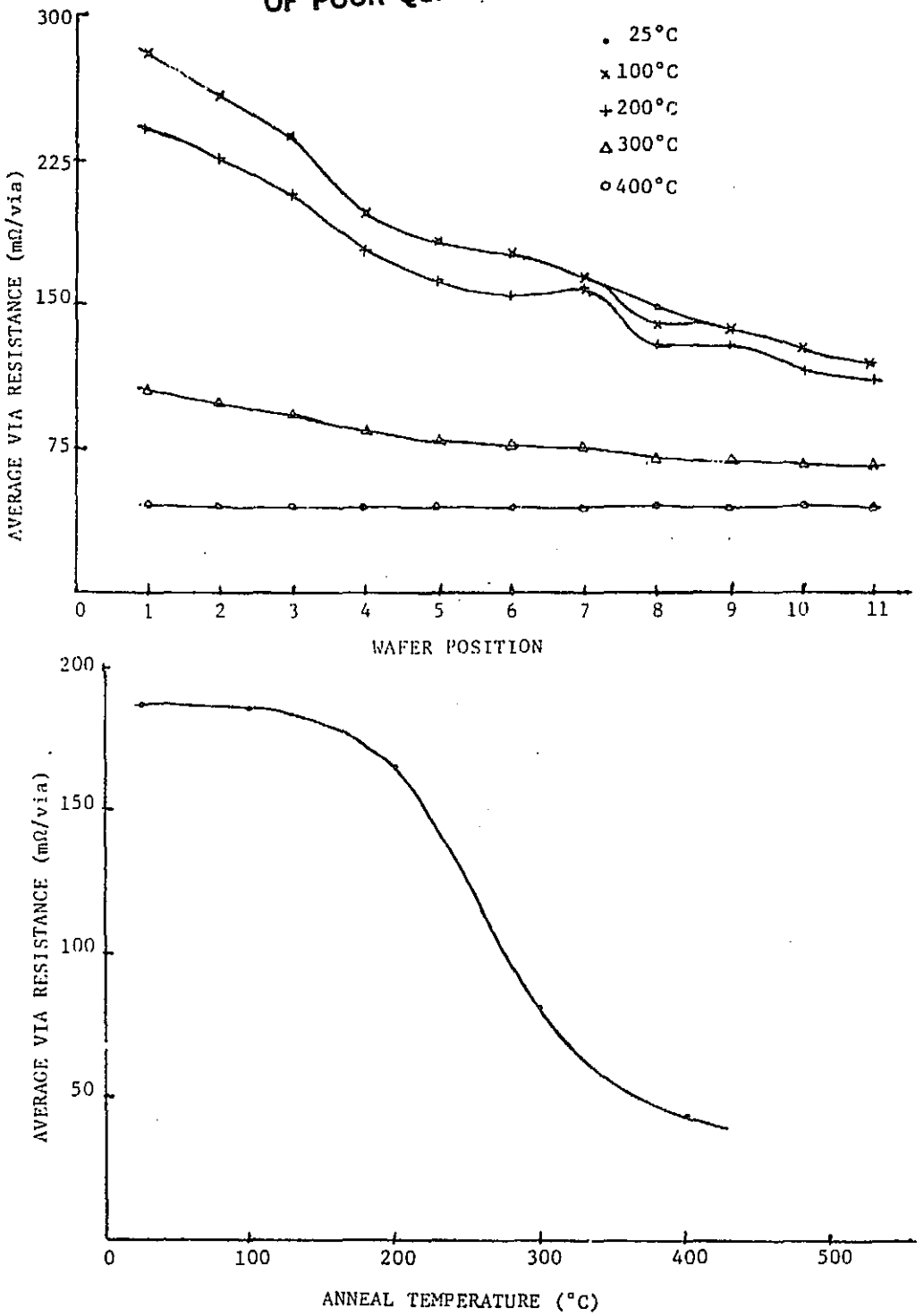


Figure 79. Wafer 8-22. The dielectric consist of 1.2 microns of Hitachi PIQ-13.

WAFER NUMBER	8-24		DIELECTRIC TYPE	2555		
CAPACITANCE (100KHZ)	15.75pf		DIELECTRIC THICKNESS	1.825microns		
1st METAL(CO) RESISTANCE	1006ohms		2nd METAL(CO) RESISTANCE	294ohms		
	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE			
	25 'C	FINAL *	25 'C	200 'C	FINAL *	
CAPACITOR	.05	.4	665	555	565	*- FINAL TEMPERATURE FOR
CROSS-OVER	330	500	550	650	540	POLYIMIDE IS 400'C
1st METAL(IF)	255	285	N/A	N/A	N/A	OTHERS 500'C
2nd METAL(IF)	410	435	N/A	N/A	N/A	(CO)- CROSS-OVER
MEASURING VOLTAGE	200	214.4				(IF)- INTERDIGITATED FINGERS
						(NO)- NORMALLY OPEN
						OPEN- R)10Megohm

	VIA CHAINS					INTERDIGITATED FINGERS	
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	1	1	1	2
OPENS	7	2	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
GOOD VIA DEFINITION, SMOOTH STEPS SOME SIGNS OF 2nd METAL LIFTING	BUBBLING IN CENTER DIE, TOP PLATE OF CAPACITOR HAS BUBBLING, DEFINITE 2nd METAL LIFTING

Table 35. Summary of measured data and visual inspection for wafer 8-24.

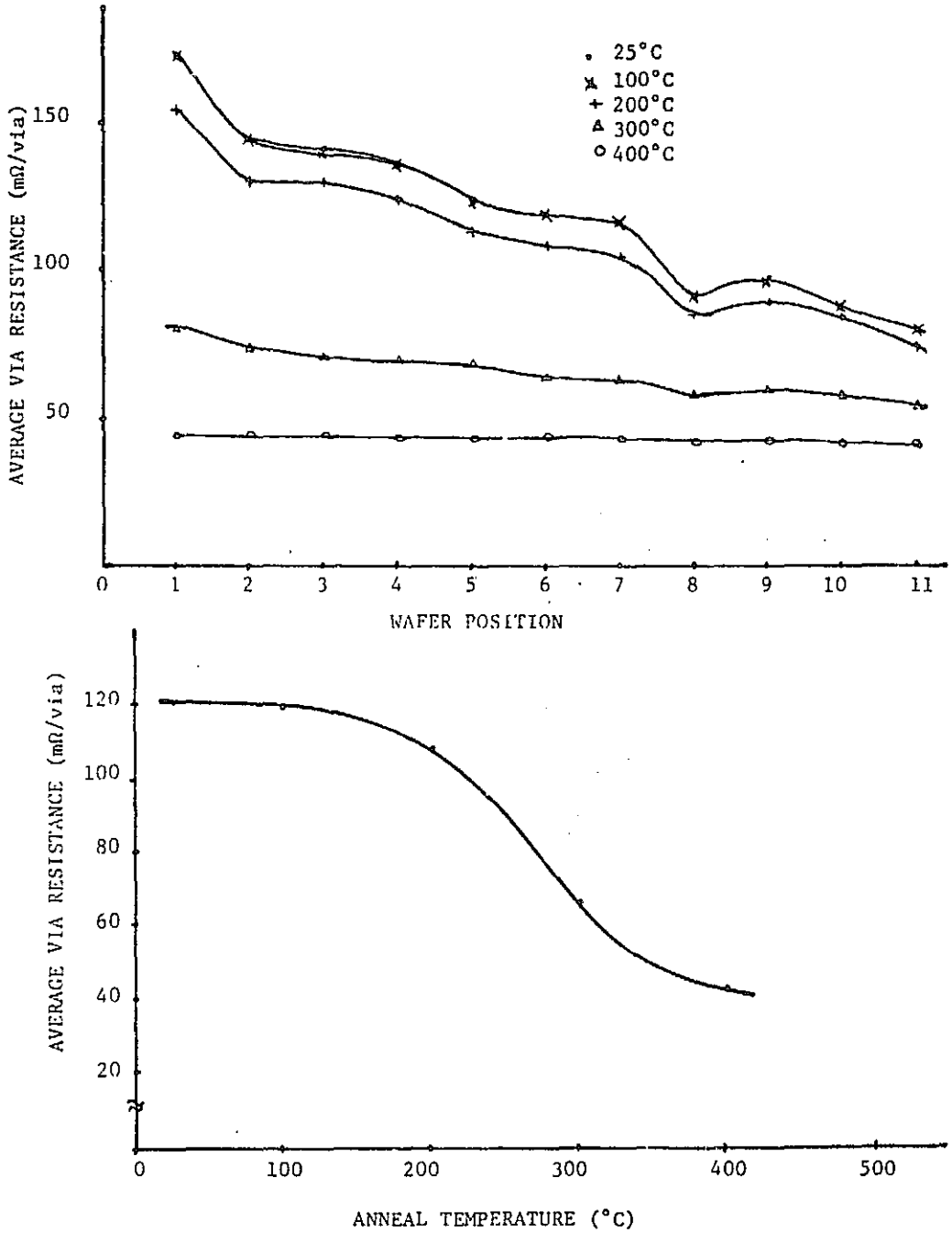


Figure 80. Wafer 8-24 . The dielectric consists of 1.5 microns thick Dupont PI-2555 polyimide.

WAFER NUMBER 8-25 DIELECTRIC TYPE 2545

CAPACITANCE (100KHZ) 18.875pf DIELECTRIC THICKNESS 1.35microns

1st METAL(CO) RESISTANCE 984ohms 2nd METAL(CO) RESISTANCE 384ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	85 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	14.9	.9	480	420	400
CROSS-OVER	200	255	400	390	230
1st METAL(IF)	120	145	N/A	N/A	N/A
2nd METAL(IF)	210	210	N/A	N/A	N/A
MEASURING VOLTAGE	142.8	142.8			

*- FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C

(CO)- CROSS-OVER

(IF)- INTERDIGITATED FINGERS

(NO)- NORMALLY OPEN

OPEN- R)10Megohm

VIA CHAINS				INTERDIGITATED FINGERS			
1080	0	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	0	0	0	0	0	0	2
OPENS	4	2	2	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
VIAS NOT WELL DEFINED, APPEARS TO BE A THICK LAYER, GOOD STEP COVERAGE	NO BUBBLIG, LOOKS GOOD

Table 36. Summary of measured data and visual inspection for wafer 8-25.

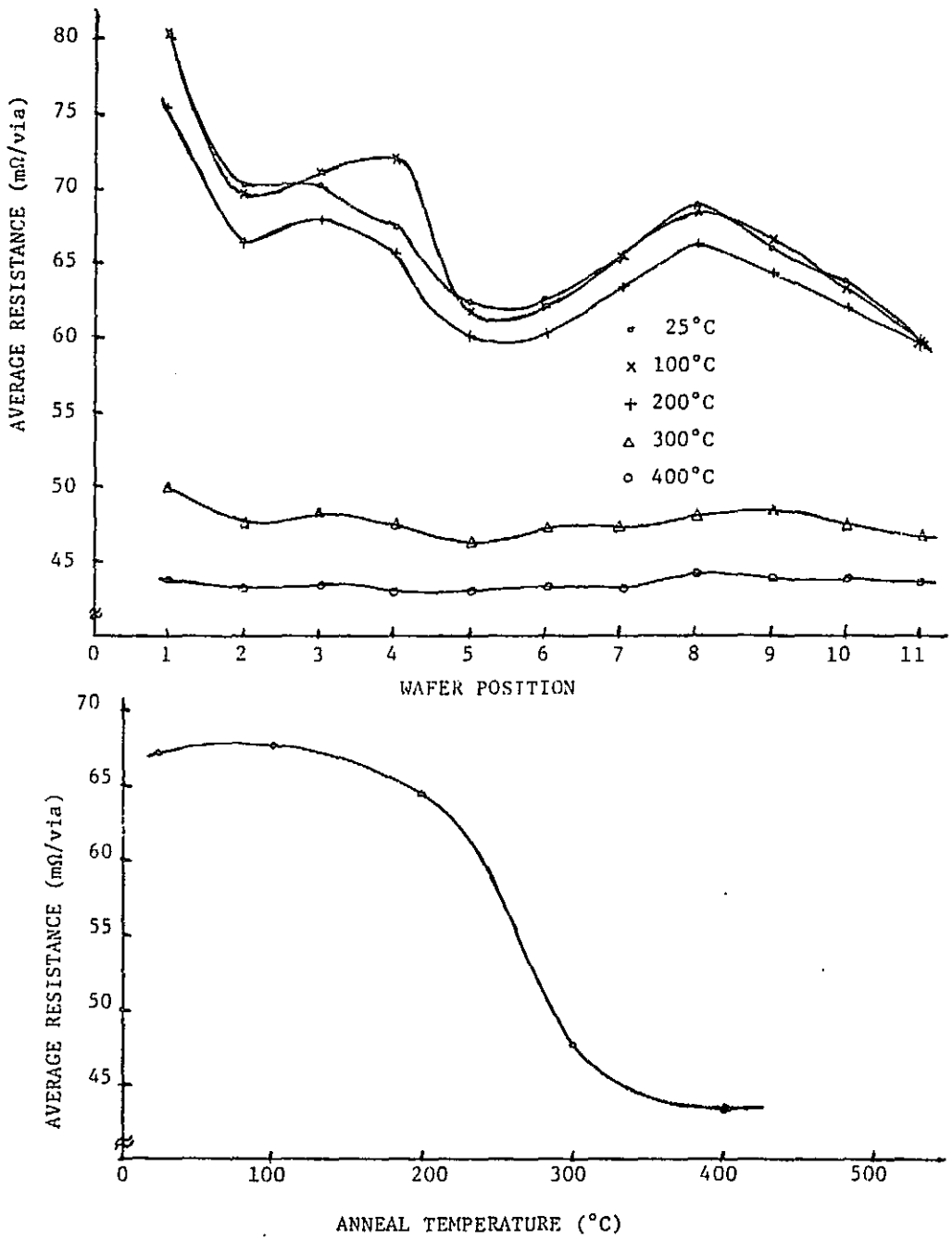


Figure 81. Wafer 8-25. The dielectric consist of 1.25 microns of Dupont PI-2545 polyimide.

WAFER NUMBER	8-13	DIELECTRIC TYPE	PIQ
CAPACITANCE (100KHZ)	14pf	DIELECTRIC THICKNESS	2.075microns
1st METAL(CO) RESISTANCE	1173ohms	2nd METAL(CO) RESISTANCE	281ohms

	LEAKAGE CURRENT(pa)		BREAKDOWN VOLTAGE		
	25 'C	FINAL *	25 'C	200 'C	FINAL *
CAPACITOR	1.5	.1	630	590	480
CROSS-OVER	190	285	640	655	560
1st METAL(IF)	135	170	N/A	N/A	N/A
2nd METAL(IF)	225	260	N/A	N/A	N/A
MEASURING VOLTAGE	214.4	214.4			

* FINAL TEMPERATURE FOR POLYIMIDE IS 400'C OTHERS 500'C
(CO)- CROSS-OVER
(IF)- INTERDIGITATED FINGERS
(NO)- NORMALLY OPEN
OPEN- R)10Megohm

	VIA CHAINS			INTERDIGITATED FINGERS			
	1000	600	400	CAPACITOR	CROSS-OVER	1st METAL	2nd METAL
SHORTS	1	0	0	0	1	0	3
OPENS	2	0	1	(NO)	(NO)	(NO)	(NO)

VISUAL INSPECTION

BEFORE ANNEALING	AFTER ANNEALING
POOR SHAPED VIAS, GOOD SLOPED SIDE WALLS, EXCELLENT STEP COVERAGE, NO SIGNS OF LIFTING	BUBBLING IN THE CENTER DIE, ALMOST ALL BREAKDOWNS OCCURRED BETWEEN PADS

Table 37. Summary of measured data and visual inspection for wafer 8-13.

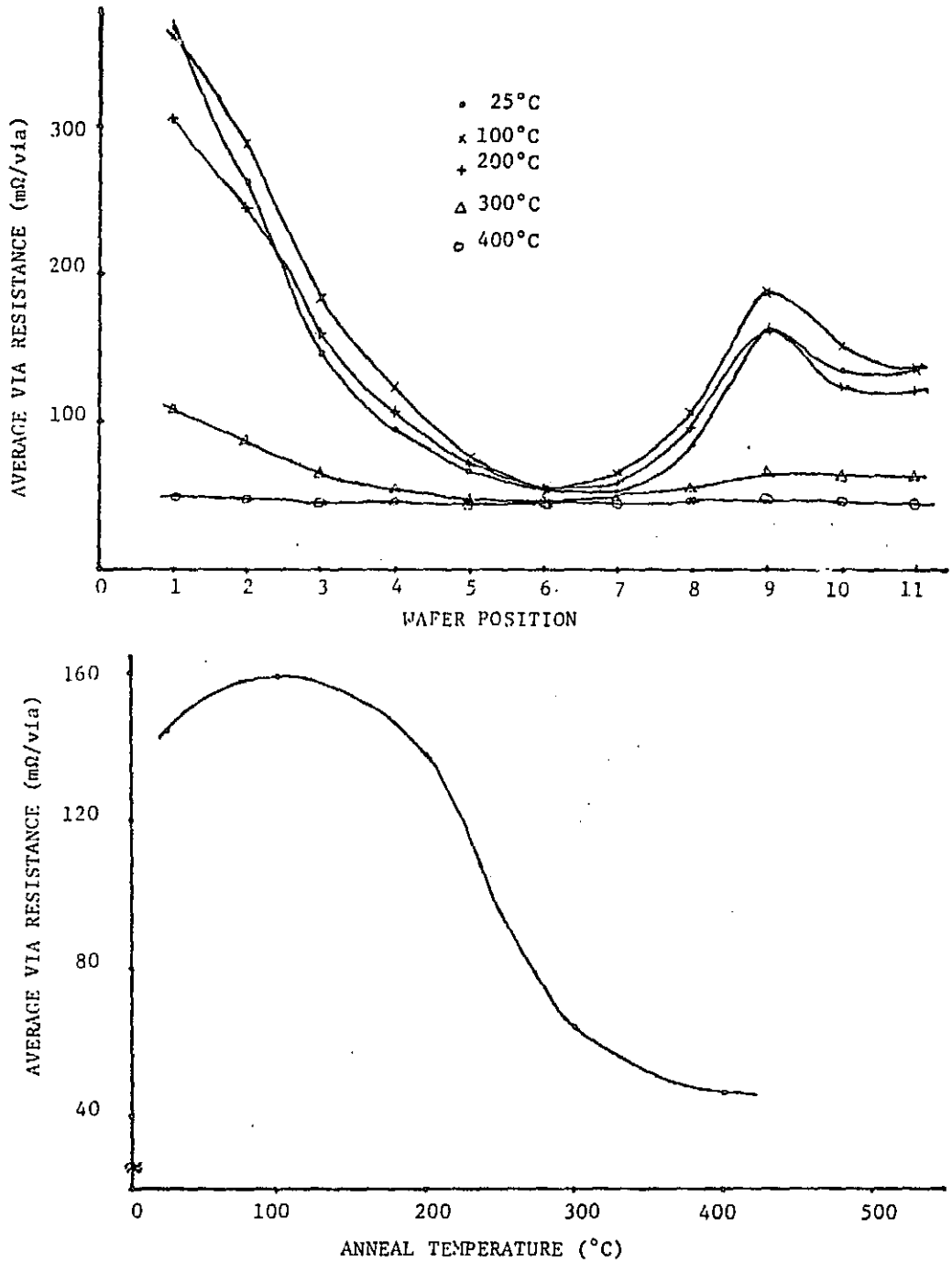


Figure 82. Wafer 8-13. The dielectric consist of 1.7 microns of Hitachi PIQ-13 polyimide.

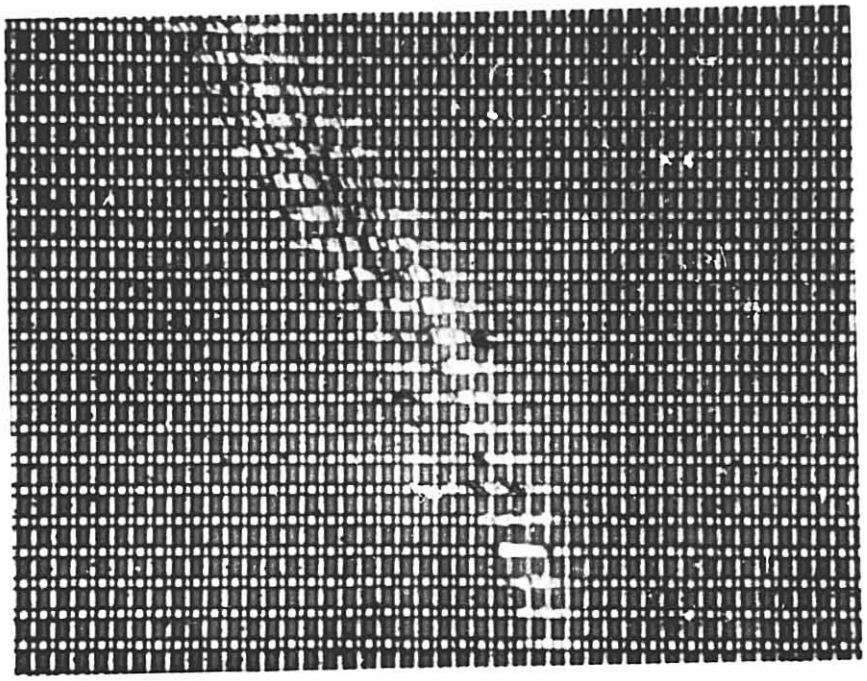


Figure 83. Wafer 9-23. 1μm PIQ. Notice the excellent second level metal adhesion to the polyimide.

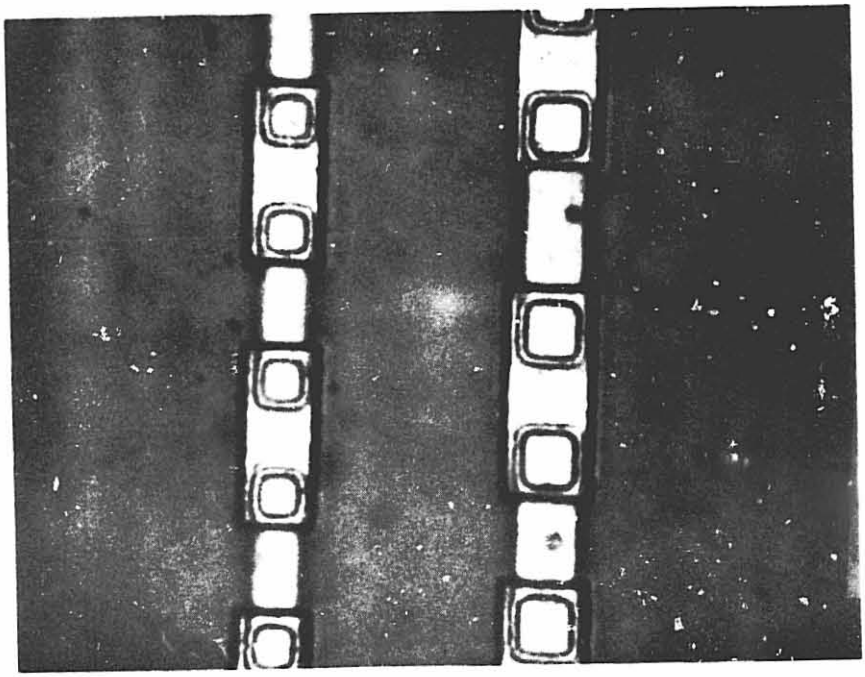


Figure 84. Wafer 9-16. 0.5 μm Dupont PI 2555. Notice both large and small via formation.

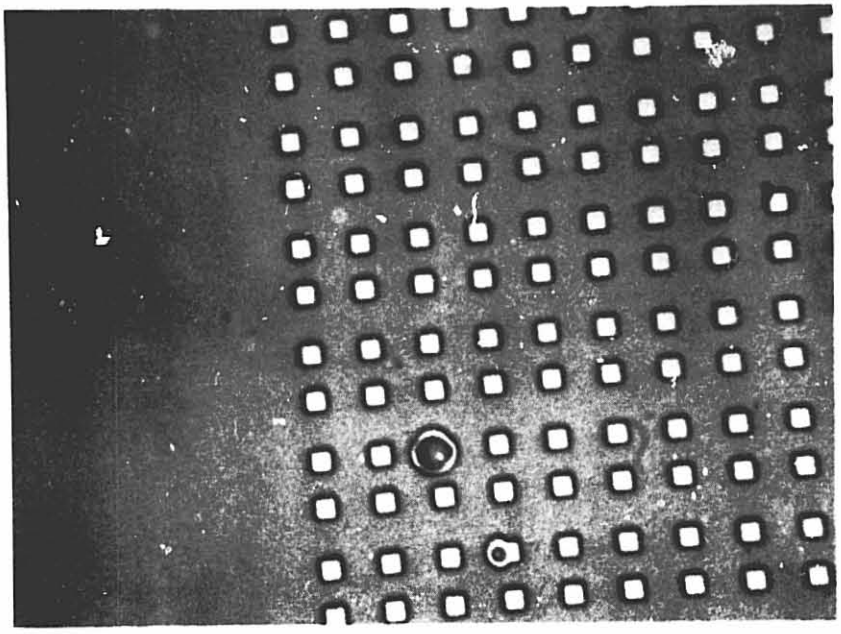


Figure 85. Dupont PI 2555 approximately 1μm thick. Notice particulates for which polyimide would not cover or adhere to. Unknown if they were on the wafer initially or in the polyimide. Also, coupler VM651 was used.

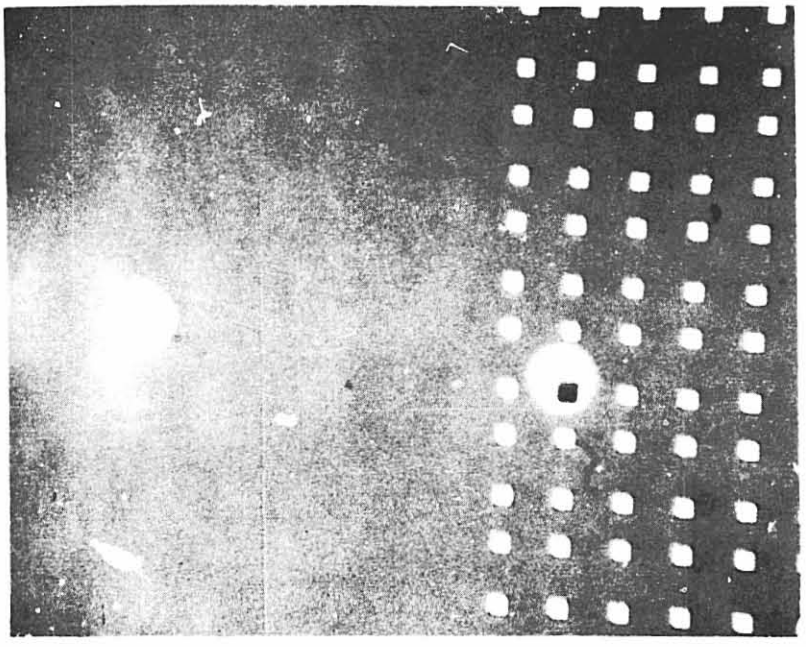


Figure 86. Dupont PI 2555. On a few wafers, light areas (yielding dark vias) were observed in the polyimide. Believe this is results of not filtering polyimide just prior to use.

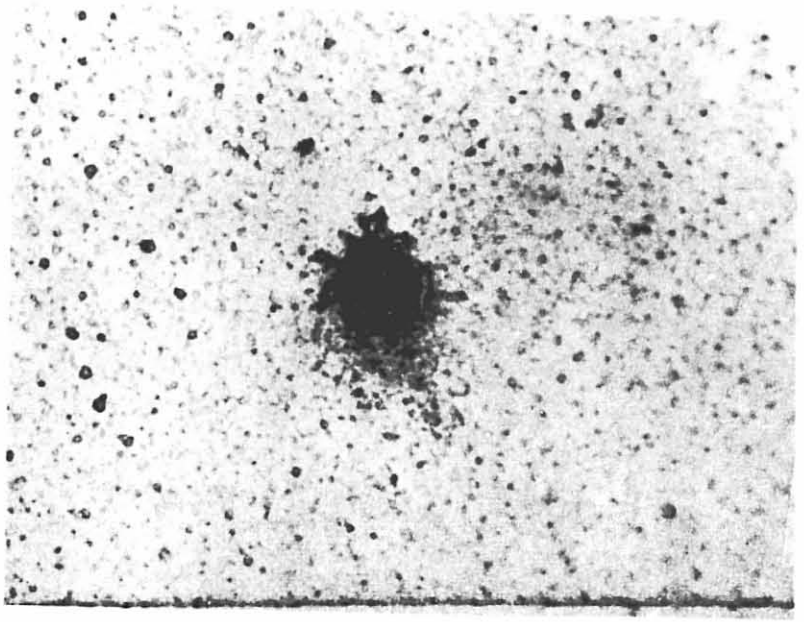


Figure 87. Wafer 8-18. 1μm PI 2555. Notice breakdown location in large capacitor.

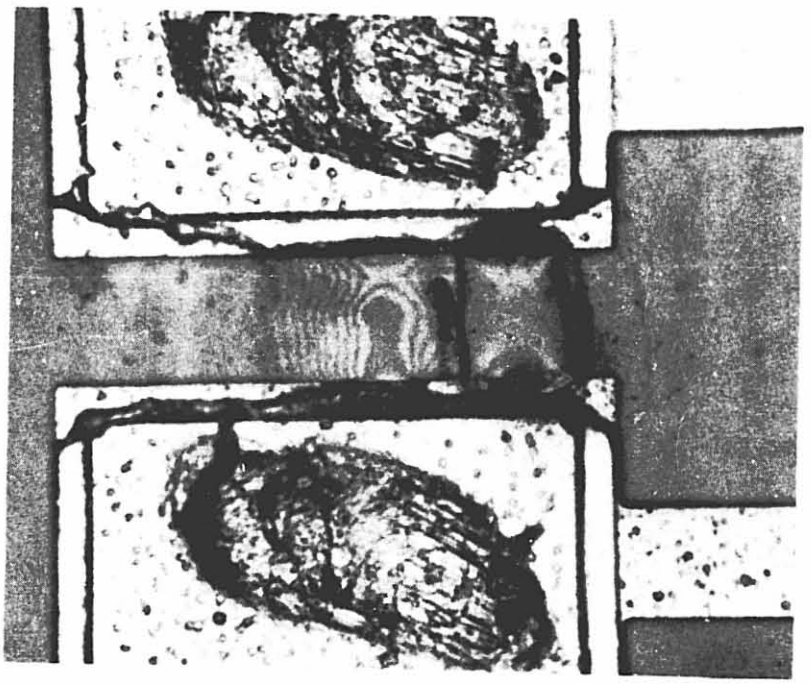


Figure 88. Wafer 8-18. Notice that occasionally, breakdown occurred between pads.

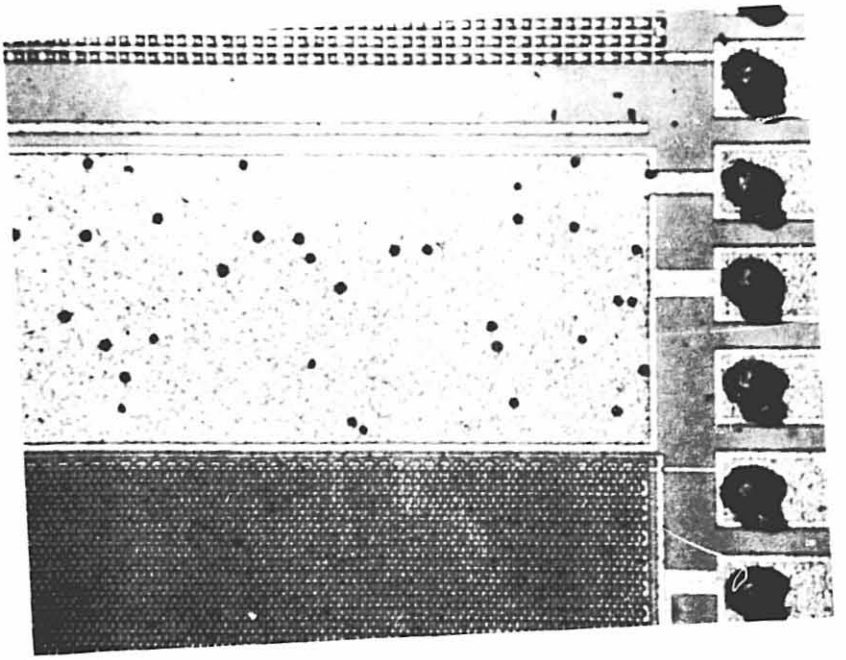


Figure 89. Wafer 9-25. 1μm PIQ. In this die, the breakdown of the capacitor experienced multiple breakdown locations as shown.

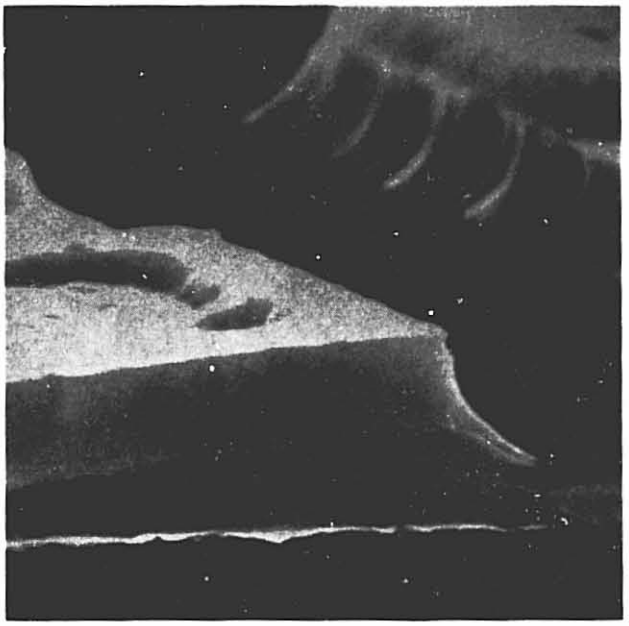


Figure 90. Via of wafer 9-13, dielectric consist of thin layer (~0.5μ) polyimide PIQ-13. Magnification is 6600X.

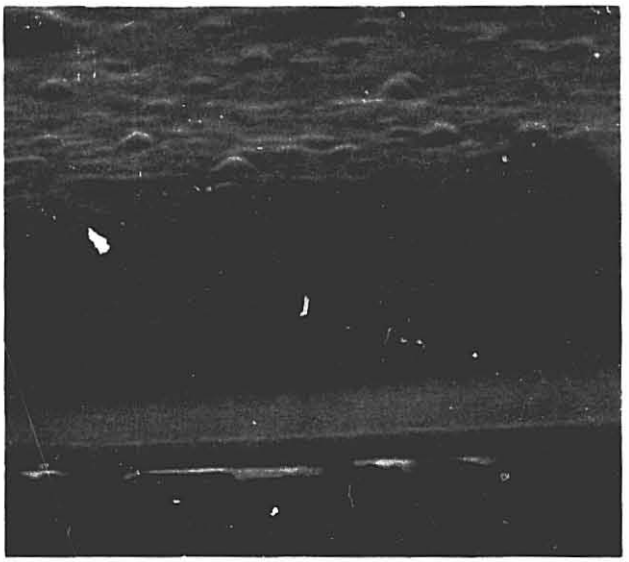


Figure 91. Cross-section of big capacitor for wafer 9-13 illustrating top layer Al/Si, PIQ and bottom layer Al/Si. Top layer metal is lifted off the polyimide in preparing the SEM sample. Magnification is 8800X.

Figure 92. Via of wafer 8-21, dielectric consist of approximately 0.8 μ polyimide PIQ-13. Magnification is 4400X.

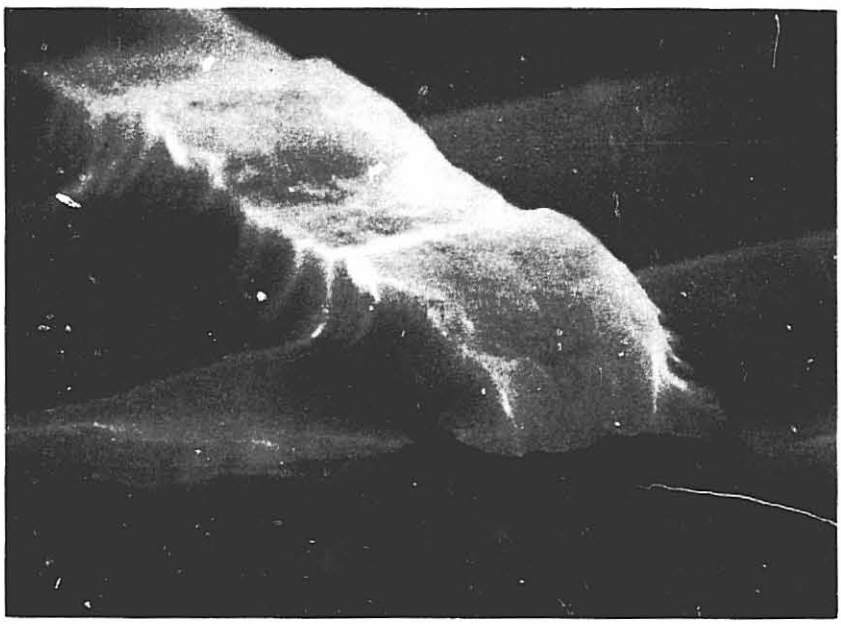


Figure 93. Cross-over of wafer 8-21. Magnification is 6600X.

Figure 94. Cross-section of big capacitor for wafer S-21 illustrating thickness of top and bottom layer metals and PIQ. Magnification is 8800X.

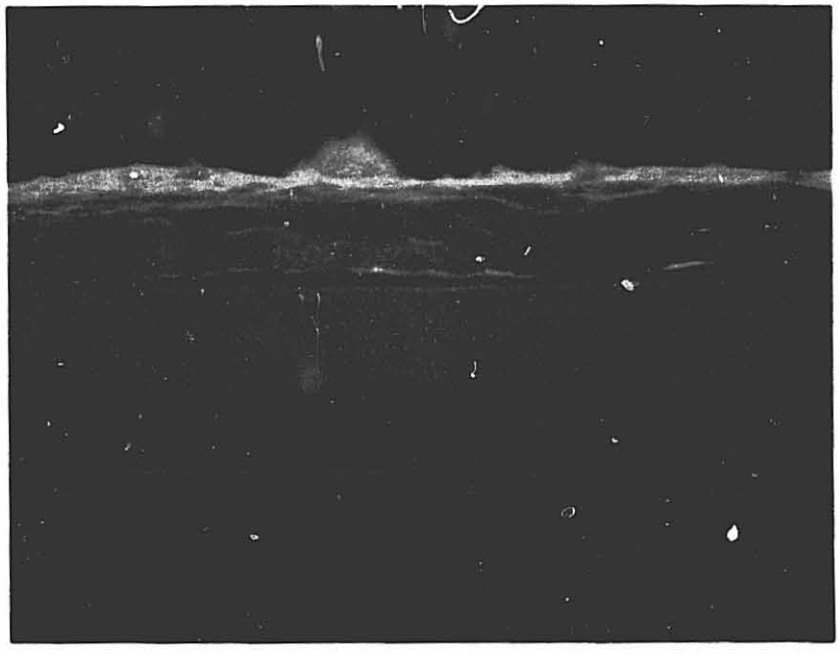


Figure 95. Cross section of big capacitor for wafer 8-1 illustrating thickness of metal layers and polyimide. Magnification is 8800X.

IV. EVALUATION OF EXPERIMENTAL DATA AND RESULTS

A. Breakdown Voltage and Leakage Currents

Breakdown voltage data was taken for all wafers prior to any temperature anneal after the 200°C anneal cycle and after the final temperature anneal. All wafers were annealed at each temperature (100, 200, 300, 400 and 500°C) for 30 minutes in nitrogen. Wafers having polyimide on them either as the sole dielectric or as a composite were final annealed at 400°C (since the polyimide dissipation factor increases above this temperature). A summary of these measured results for the no temperature and final temperature anneal cases are presented in Table 38. Also, a pictorial representation of the relative magnitudes are presented in Figures 96 through 99 for both cross-over and capacitor patterns.

Also summarized in Table 38 is the measured leakage current data taken with 142 volts applied to the capacitor, cross-over and first and second metal levels interdigitated finger patterns. It should be noted that leakage currents were taken at several applied voltages. The behavior of dielectric current as a function of applied voltage at an elevated temperature (100°C) is shown in Figure 100. Here, the linear I-V dependence is somewhat surprising since it is reported that many dielectrics behave linearly in a $V^{\frac{1}{2}}$ vs. ln(I) fashion.

WAFER	DIELECTRIC THICKNESS (microns)	BREAKDOWN VOLTAGE (volts)				MEASURED LEAKAGE CURRENT Applied Voltage = 142 volts (pico-amperes)							
		T= 25°C		T = 500°C		T = 25°C				T = 400/500°C			
		C	C.O.	C	C.O.	C	C.O.	1-I.F	2-I.F	C	C.O.	I-I.F	2-I.F
1-7	0.98	-	-	160	470	-	-	-	-	0.5	230	135	205
9-2	1.1	590	610	600	575	31.9	585	310	700	2.5	57	28	42
9-8	1.4	335	45[illegible]	355	340	66.2	810	320	635	8.0	182	93	157
2-22	1.0	610	585	530	560	4.2	530	590	740	0.45	172	97	157
2-8	1.0	450	550	580	520	11.7	53	53	82	0.12	142	82	128
2-15	1.2	555	585	560	560	4.7	60	32	50	0.3	83	47	72
2-2	1.3	620	660	580	575	0.83	42	27	42	0.15	95	57	83
7-2	0.9	480	400	355	345	6.4	230	110	165	9.1	350	110	155
7-13	0.8	510	490	330	345	0.7	85	50	75	1.8	330	80	150
3-23	0.95	510	460	540	541	0.33	123	77	127	0.1	150	87	148
3-9	1.1	350	520	540	460	7.0	215	275	320	0.17	300	170	260
3-6	1.1	545	465	530	495	3.5	310	95	145	0.1	265	155	220
7-25	1.1	540	545	600	530	3.2	53	30	48	1.3	97	53	83
7-15	0.8	300	520	330	400	26	210	380	170	2385	10K	700	650
7-14	0.85	500	450	310	390	14.9	590	365	615	4.15	227	112	200
3-25	0.8	500	510	355	480	3.9	105	50	97	0.9	67	37	102
5-14	0.35	s.c.	s.c.	s.c.	s.c.	s.c.	s.c.	195	115	-	-	7350	16K
5-21	1.0	260	330	220	355	9.6	176	352	256	240	1450	1150	1400
8-3	0.7	230	135	180	135	92	768	112	224	17K	1450	800	1200
5-3	1.0	520	400	450	365	7.0	3400	635	560	12.2	1700	200	315
5-12	1.1	590	525	525	400	11.4	147	43	77	0.3	152	83	122
8-10	0.7	410	310	400	270	70.3	740	60	100	0.6	240	135	220
9-16	1.0	475	290	310	350	10.7	170	95	145	0.2	285	165	240
9-25	0.8	260	290	200	190	10	176	112	208	1025	450	270	350
8-18	1.5	620	635	565	515	17.5	875	990	1300	0.15	187	105	167
8-20	1.1	320	300	320	310	52.1	245	115	215	1.0	290	160	236
8-22	1.2	485	480	470	470	7.1	135	75	130	1.0	275	155	230
8-24	1.5	665	550	565	540	0.8	115	75	175	0.35	167	95	145
8-25	1.25	480	400	400	230	14.9	200	120	210	0.9	255	145	210
8-13	1.7	630	640	480	560	0.5	63	45	75	0.1	95	57	87

Table 38. Summary of breakdown voltages and leakage currents for capacitor (C), cross-over (C.O.) and both levels of interdigitated fingers (I.F.).

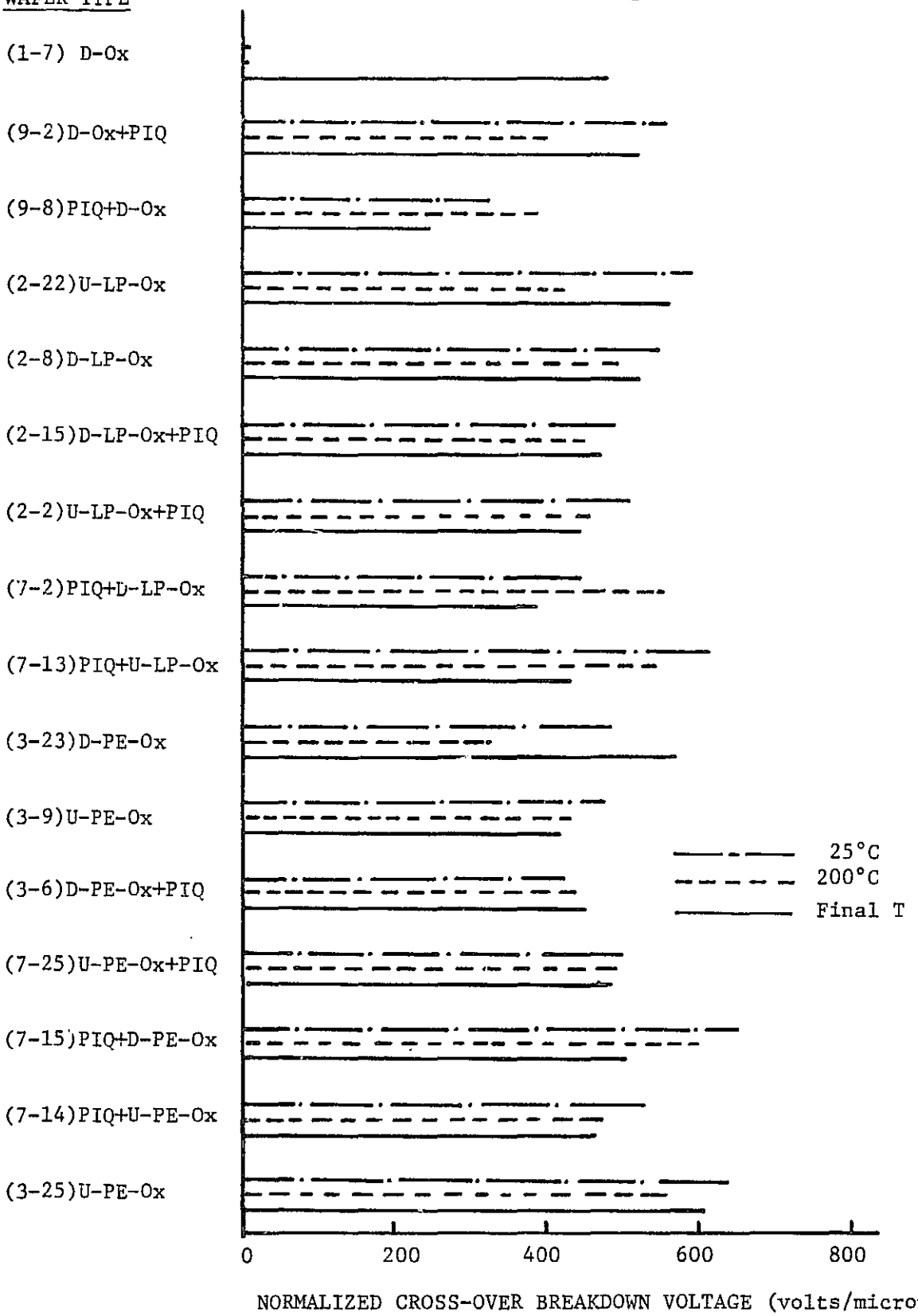


Figure 96. A plot of normalized breakdown voltages for cross-overs as a function of wafer type for three temperature anneal conditions: 25°C-no anneal; 200°C-annealed for 30 minutes in nitrogen; Final T-annealed for 30 minutes at 400°C for polyimides, 500°C for all other dielectrics.

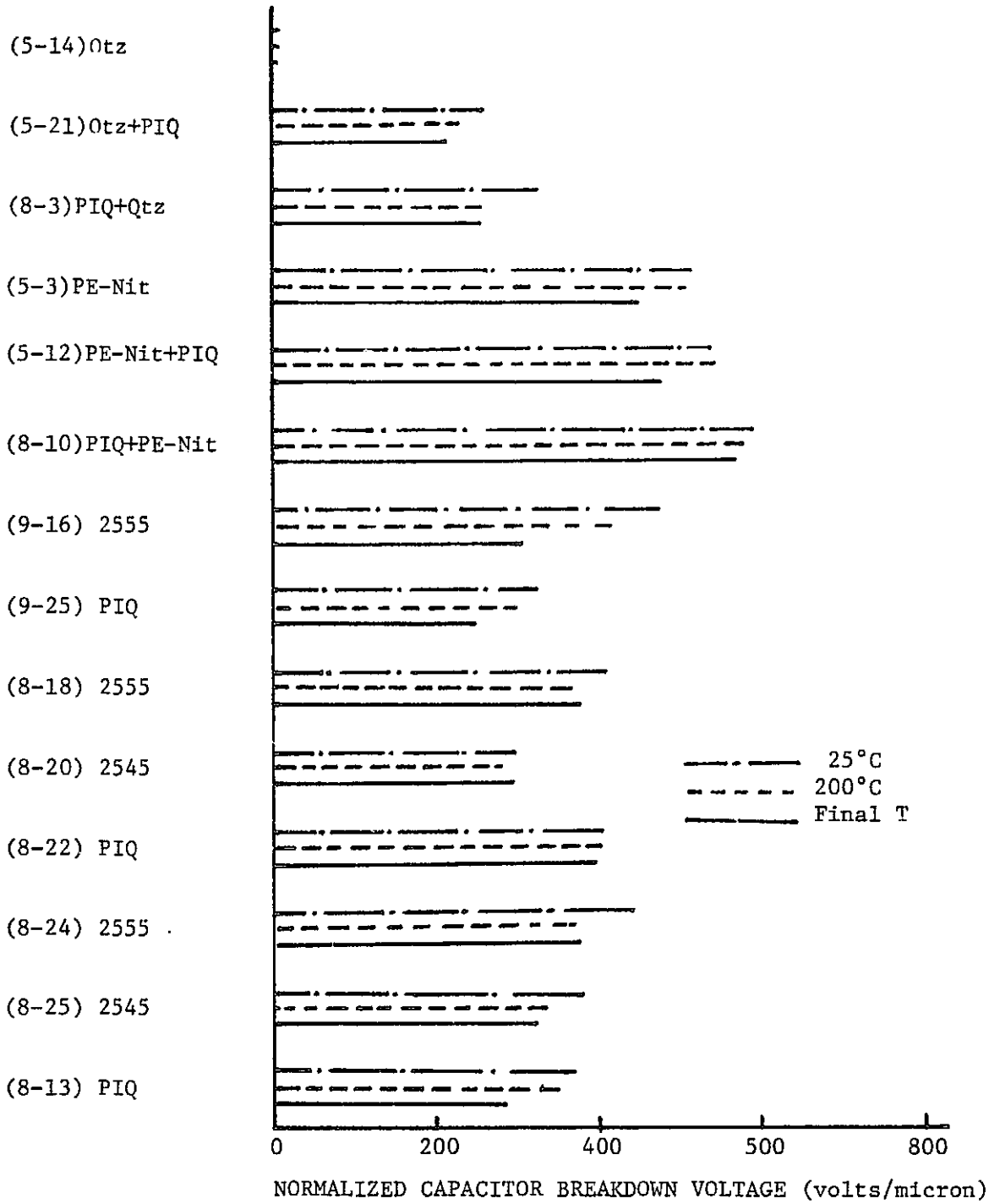


Figure 97. A plot of normalized breakdown voltages for capacitors as a function of wafer type for three temperature anneal conditions: 25°C - no anneal; 200°C-anneal for 30 minutes in nitrogen; Final T - anneal for 30 minutes at 400°C for polyimides, 500°C for all other dielectrics.

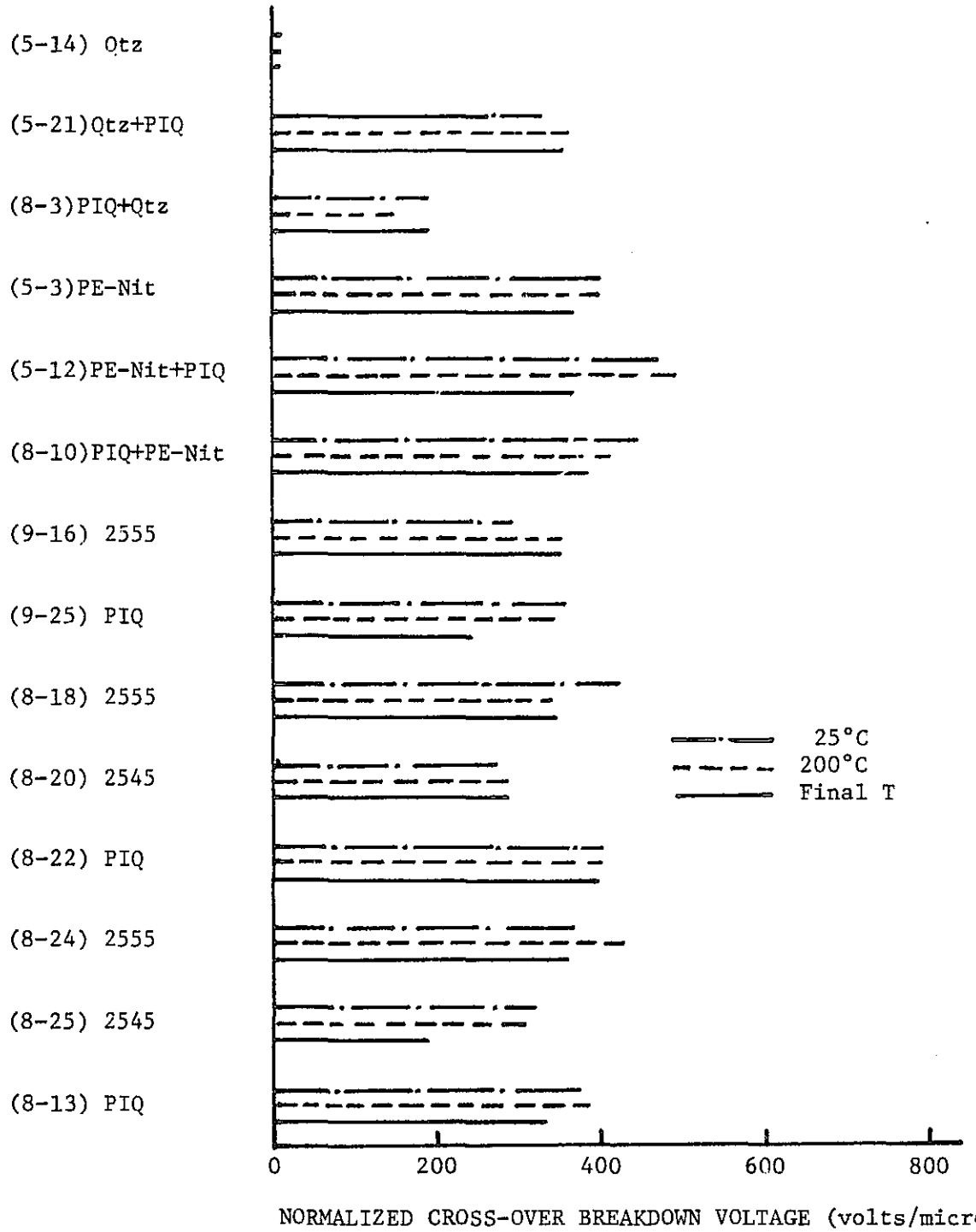


Figure 98. A plot of normalized breakdown voltages for cross-overs as a function of wafer type for three temperature anneal conditions: 250°C-no anneal, 200°C-annealed for 30 minutes in nitrogen; Final T-annealed for 30 minutes at 400°C for polyimides, 500°C for all other dielectrics.

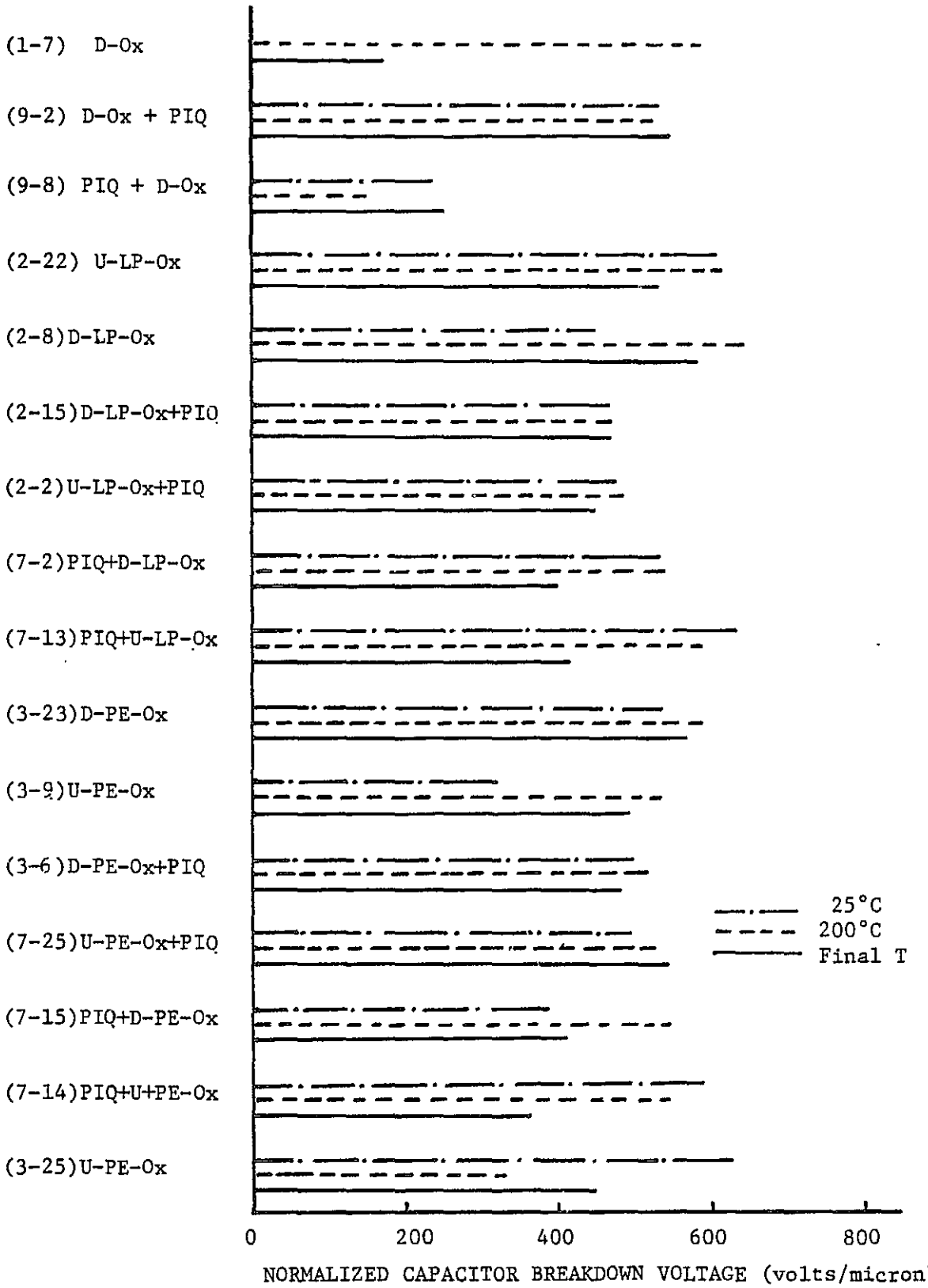


Figure 99. A plot of normalized breakdown voltages for capacitors as a function of wafer type for three temperature anneal conditions: 25°C-no anneal; 200°C-anneal for 30 minutes in nitrogen; Final T-anneal for 30 minutes at 400°C for polyimides, 500°C for all other dielectrics.

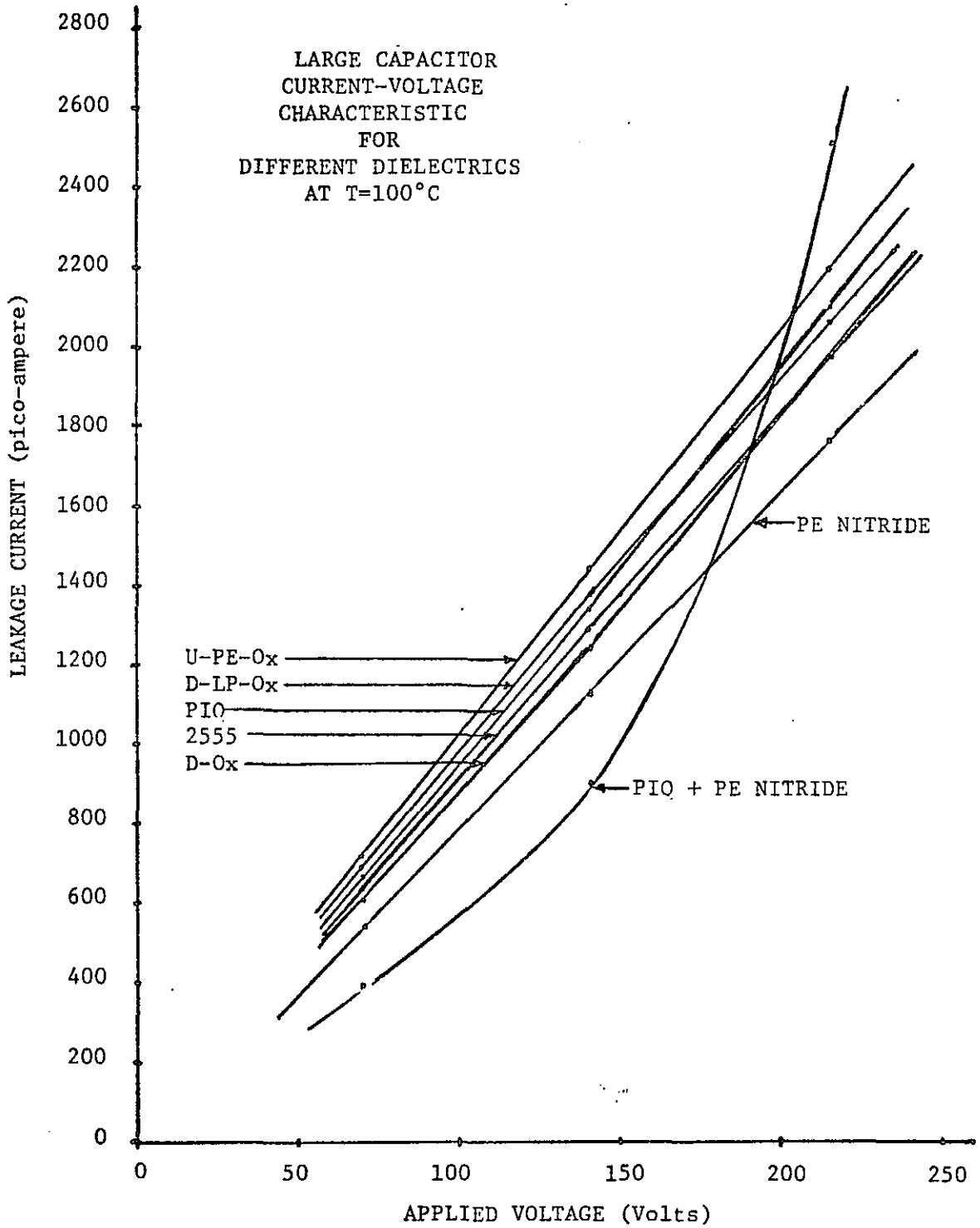
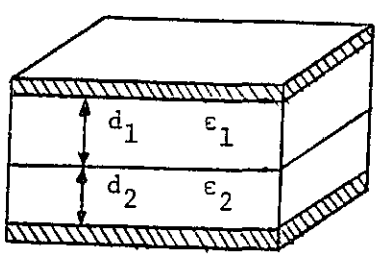


Figure 100. Measured value of leakage current as a function of voltage at T = 100°C for several dielectric types.

B. Dielectric Thicknesses

Sample calculation of total dielectric thickness for two different dielectric composit wafers.

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \quad \text{where} \quad C = \frac{\varepsilon_o \varepsilon_r A}{d}$$



$$\varepsilon_o = 8.854 \times 10^{-18} \text{ f/}\mu$$

$$A = 770{,}625 \mu m^2$$

thus

$$d_1 = \varepsilon_{r_1} \left[\frac{\varepsilon_o A}{C_T} - \frac{d_2}{\varepsilon_{r_2}} \right]$$

and assume

TYPE	ε_r
atmospheric CVD oxide	4.2
LPCVD oxide	5.2
plasma enhanced oxide	4.7
sputtered quartz	4.3
plasma enhanced nitride	7.2
polyimide	3.6

Calculation of wafer 9-2, polyimide deposited over atmospheric CVD oxide. The oxide was measured accurately using the nanospec, however polyimide thickness not accurately known due to

t"< t' -planarizing effect

$C_{measured} = 23.3$ pf

$d_{oxide} = d_2 = 0.43$ µm

$$d_1 = \varepsilon_{r_1} \left[\frac{\varepsilon_o A}{C_T} - \frac{d_2}{\varepsilon_{r_2}} \right]$$

$$= 3.6 \left[\frac{(8.854 \times 10^{-18} f/\mu)(7.70625 \times 10^{5} \mu m^2)}{23.3 \times 10^{-12} f} - \frac{0.43 \mu m}{4.2} \right]$$

$$= 0.685 \mu m$$

Therefore $d_T = d_1 + d_2 = 0.685 + 0.43 = 1.1 \mu m$

The dielectric thickness for most test samples was determined by a combination of nanospec, alpha step and capacitance measurement data. With the polyimide materials, the thickness of the dielectric over first level metal patterns was found to be 75-80 percent of the thickness over the substrate resulting from its planarizing quality. Hence a combination of SEM analysis and capacitance measurements rendered the best results for these dielectrics.

A summary of dielectric thicknesses for the wafers tested is given in Table 39. Also in this table is the number of via open circuits and capacitor, cross-over and interdigitated finger short circuit.

WAFER	DIELECTRIC THICKNESS (microns)			VIA'S OPEN CIRCUIT ( )-Short Circuit			SHORT CIRCUITS			
	d_1 bottom	d_2 top	d_T total	1000	600	400	C	C.O.	1-IF	2-IF
1-7	0.98		0.98	0	0	0(1)	3	5	1	0
9-2	0.43	0.67	1.1	All	All	All	0	0	0	8
9-8	0.92	0.48	1.4	All	All	75	0	0	2	3
2-22	1.0		1.0	71	64	63	2	0	1	1
2-8	1.0		1.0	71	59	65	4	4	2	1
2-15	0.25	0.95	1.2	4(1)	2	4	1	0	3	6
2-2	0.25	1.05	1.3	1	1	1	0	0	0	4
7-2	0.65	0.25	0.9	2(2)	3(1)	1	1	2	0	2
7-13	0.55	0.25	0.8	0(3)	2	0	2	2	0	1
3-23	0.95		0.95	1(4)	0(4)	0(5)	2	34	0	0
3-9	1.1		1.1	14(2)	10	8	23	31	0	1
3-6	0.25	0.85	1.1	2	0	1	1	1	2	1
7-25	0.26	0.84	1.1	1(1)	4	1(1)	2	1	0	1
7-15	0.54	0.26	0.8	All	All	All	0	2	1	2
7-14	0.55	0.30	0.85	All	All	All	2	0	1	5
3-25	0.80		0.80	1(1)	2	1	27	55	1	1
5-14	0.35		0.35	0	0	0(1)	All	All	0	1
5-21	0.11	0.89	1.0	2(1)	0(1)	1(1)	2	2	0	1
8-3	0.59	0.11	0.7	1	0	0	3	2	0	2
5-3	1.0		1.0	0	1	1	11	20	0	1
5-12	0.25		1.1	0	0	0	0	0	0	1
8-10	0.45	0.85	0.7	1	0(1)	0	0	1	0	1
9-16	1.0	0.25	1.0	0	0	0	0	0	0	1
9-25	0.8		0.8	1	1	1(1)	1	0	0	1
8-18	1.5		1.5	8	12	13	0	1	1	1
8-20	1.1		1.1	2	1	4	0	0	1	2
8-22	1.2		1.2	1	0	0	0	0	0	1
8-24	1.5		1.5	7	2	1	1	1	1	2
8-25	1.25		1.25	4	2	2	0	0	0	2
8-13	1.7		1.7	2(1)	0	1	0	1	0	3

Table 39. A summary of dielectric thicknesses, the number of via open-circuits and the number of capacitor (C), cross-over (C.O.) and interdigitated fingers (I.F.) short circuits.

C. A Figure of Merit for Dielectrics

In order to compare the various types of dielectrics tested in order to find the optimum dielectric for double layer metal processes, a figure of merit had to be derived. This figure of merit should include the following dielectric characteristics:

- high breakdown voltage for both capacitor and cross-over structures per unit thickness (maximum electric field strength).
- high dielectric resistance (as measured by leakage current for an applied voltage) per unit thickness
- low number of short circuits measured between metal layers for capacitor and cross-over structures as well as between interdigitated fingers for each metal level
- high interface dielectric resistance (as measured between interdigitated fingers for each metal level)

Taking all of these desirable parameters into account, a dielectric and a comprehensive dielectric figure of merit (CDFM) have been defined (see next subsections). Based on these definitions, calculations for each dielectric have been undertaken and the results shown in Tables 40 and 41 for no anneal and final anneal cases. In addition, representation of the top ten dielectrics as per their CDFM value are shown in Figures 101 through 103. Figure 103 represents the results if two micron thick polyimide (twice the normalized breakdown voltage and dielectric resistance) are compared to one micron thick dielectric for all others considered.

C1 - DIELECTRIC FIGURE OF MERIT - D.F.M.

$$D.F.M. = [NOR\text{-}B.V.][NOR\text{-}R_D][1/N\ s.c.]$$

where

$NOR\text{-}B.V.$ = Normalized Breakdown Voltage (volts/micron)

$$= \frac{\text{Measured Breakdown Voltage}}{\text{Dielectric Thickness}} = \frac{B.V.}{t}$$

= Maximum Electric Field Strength

$NOR\text{-}R_D$ = Normalized Dielectric Resistance (ohms/micron)

$$= \frac{V_{applied}}{I_{leakage}} \cdot \frac{1}{\text{Dielectric Thickness}} = \frac{V_a}{I_\ell} \cdot \frac{1}{t}$$

$\frac{1}{N_{s.c.}}$ = A degradation in DFM by up to 50% due to the measured number of short circuits (s.c.) per wafer (76 die) in capacitors or cross-overs.

$$= 1 - 6.58\times10^{-3}(\#s.c.)$$

C2 - COMPREHENSIVE DIELECTRIC FIGURE OF MERIT - C.D.F.M.

$$C.D.F.M. = [\text{Capacitor D.F.M.}][\text{Cross-Over D.F.M.}]\ R_{I.F.}$$

where

$R_{I.F.}$ = Interface dielectric resistance measured between interdigitated fingers (I.F.) for both first level ($R_{I.F.-1}$) and second level ($R_{I.F.-2}$) metal layers.

$$= (R_{I.F.-1})(R_{I.F.-2})\ (1/R_{IF\text{-}s.c.})$$

and

$\frac{1}{R_{IF\ -s.c.}}$ = A degradation in $R_{I.F.}$ by up to 50% due to the sum of the measured number of short circuits per wafer (76 die) in the first and second level metal interdigitated finger test pattern.

$$= 1\text{-}6.58\times10^{-3}(\#s.c.\text{ in first and second level I.F.'s})$$

C3 - SAMPLE CALCULATION OF C.D.F.M.

Wafer 2-22 After Final Anneal Temperature

C.D.F.M. = (Capacitor D.F.M.)(Cross-Over D.F.M.)$R_{I.F.}$

where

Capacitor D.F.M. = (NOR-B.V.)(NOR-R_D)(1/$C_{s.c.}$)

and

measured B.V. = 530 volts

$I_{leakage}$ = 0.45 pico-amp for 142 volts applied

thickness = 1.0μm

$$\text{NOR-B.V.} = \frac{530 \text{ volts}}{1.0 \ \mu m} = 530 \text{ volts}/\mu m$$

$$\text{NOR-}R_D = \frac{V_{applied}}{I_{leakage}} \frac{1}{t} = \frac{142 \text{ volts}}{0.45pA} \frac{1}{1.0\mu m} = 315.6\text{x}10^{12} \text{ohms}/\mu m$$

Number of capacitor short circuits in 76 die = 2

$$1/C_{s.c.} = \frac{1}{100}\left[50\left(\frac{76-X}{76}\right) + 50\right] = 1-6.579\text{x}10^{-3}(\#s.c.)$$

$$= 1-6.58\text{x}10^{-3}(2) = 0.987$$

Therefore:

$$\text{Capacitor D.F.M.} = (530 \text{ volts}/\mu m)(315.6\text{x}10^{12}\text{ohm}/\mu m)(0.987)$$

$$= 165.1\text{x}10^{15} \text{ volt-ohm}/\mu m^2$$

Also

Cross-over D.F.M. = (NOR-B.V.)(NOR-R_D)(1/$CO_{s.c.}$)

measured B.V. = 560 volts

$I_{leakage}$ = 172 pA

thickness = 1.0μm

$$\text{NOR-B.V.} = \frac{560 \text{ volts}}{1\ \mu m} = 560 \text{ volts}/\mu m$$

$$\text{NOR-}R_D = \frac{142 \text{ volts}}{172 \text{ pA}} \quad \frac{1}{1.0\mu m} = 0.826 \times 10^{12} \text{ ohm}/\mu m$$

Number of cross-over short circuits in 76 die = 0

$$1/CO_{s.c.} = 1$$

and

$$\text{Cross-over D.F.M.} = (560 \text{ volts}/\mu m)(0.826 \times 10^{12} \text{ohm}/\mu m)(1.0)$$

$$= 462.56 \times 10^{12} \text{ volt-ohm}/\mu m^2$$

Now

$$R_{I.F.} = (R_{IF-1})(R_{IF-2})(1/R_{IF-s.c.})$$

Measured leakage current for 1st level = 97 pA

Measured leakage current for 2nd level = 157 pA

$$(R_{IF-1})(R_{IF-2}) = (\frac{142 \text{ volts}}{97 \text{ pA}})(\frac{142 \text{ volts}}{157 \text{ pA}}) = 1.324 \times 10^{24} \text{ohm}^2$$

Number of interdigitated finger short circuit for first level metal is 1, and for second level metal 1; total for both levels 2

$$1/R_{IF-s.c.} = 1-6.58 \times 10^{-3}(2) = 0.987$$

Thus

$$R_{I.F.} = (1.324 \times 10^{24})(0.987) = 1.307 \times 10^{24} \text{ohm}^2$$

$$\text{C.D.F.M.} = [(165.1 \times 10^{15} \text{ volt-ohm}/\mu m^2)(462.56 \times 10^{12} \text{volt-ohm}/\mu m^2)$$

$$(1.307 \times 10^{24} \text{ohm}^2)] = 9,981 \times 10^{52} \quad \frac{\text{volts}^2 \text{ohms}^4}{\mu m 4}$$

WAFER	CAPACITOR (NO ANNEAL)				CROSS-OVER (NO ANNEAL)				INTERDIGITATED FINGERS			
	R_{NOR} $X10^{11}$	BV_{NOR}	#s.c.	DFM $X10^{14}$	R_{NOR} $X10^{11}$	BV_{NOR}	#s.c.	DFM $X10^{14}$	#s.c. 1-I.F.	#s.c. 2-I.F.	R_{IF} $X10^{22}$	CDVM $X10^{55}$
1-7	-	-	3	-	-	-	5	-	1	0	-	-
9-2	40.5	536	0	22	2.21	555	0	1.23	0	8	8.8	-0
9-8	15.3	239	0	3.7	1.25	325	0	40.6	2	3	9.6	0.01
2-22	338	610	2	204	2.68	585	0	157	1	1	4.6	1.5
2-8	121	450	4	53	26.8	550	4	1436	2	1	454	345
2-15	252	463	1	116	19.7	488	0	961	3	6	1186	1322
2-2	1316	477	0	628	26	508	0	1321	0	4	1732	14367
7-2	247	533	1	130	6.9	444	2	301	0	2	110	43
7-13	2536	638	2	1596	21	612	2	1263	0	1	534	10760
3-23	4530	537	2	2401	12	484	34	455	0	0	206	2250
3-9	184	318	23	49.3	6	472	31	225	0	1	23	26
3-6	369	495	1	181	4.2	423	1	175	2	1	144	46
7-25	403	491	2	195	24	495	1	1197	0	1	1390	3246
7-15	68	385	0	26.5	8.5	650	2	548	1	2	31	4.5
7-14	112	588	2	64	2.8	529	0	150	1	5	9	0.9
3-25	453	625	27	234	16.9	637	55	686	1	1	410	658
5-14	0	-	76	-	0	s.c.	76	-	0	1	89	-
5-21	148	260	2	38	8.1	330	2	263	0	1	22	2.2
8-3	22	328	3	7	2.6	193	2	51	0	2	80	0.3
5-3	203	520	11	98	0.4	400	20	14.6	0	1	5	-0
5-12	113	536	0	61	8.8	477	0	421	0	1	604	155
8-10	29	586	0	17	2.7	443	1	121	0	1	334	7
9-16	133	475	0	63	8.3	290	0	242	0	1	145	22
9-25	178	325	1	57	10	363	0	367	0	1	86	18
8-18	54	413	0	22	1.1	423	1	45	1	1	1.5	0.01
8-20	25	291	0	7.3	5.3	273	0	144	1	2	80	0.8
8-22	168	404	0	68	8.8	400	0	351	0	1	205	49
8-24	1183	443	1	520	8.2	367	1	300	1	2	150	234
8-25	76	384	0	29	5.7	320	0	182	0	2	79	4
8-13	1671	371	0	620	13.2	376	1	495	0	3	585	1795

Table 40. Calculated values of dielectric figure of merits (D.F.M.) and the comprehensive dielectric figure of merit (C.D.F.M.) for all wafers tested prior to temperature annealing.

WAFER	CAPACITOR (FINAL ANNEAL TEMP.)				CROSS-OVER (FINAL ANNEAL TEMP.)				INTERDIGITATED FINGERS				2μm THICK POLY-IMIDE
	R_{NOR} $X10^{12}$	BV_{NOR}	#s.c.	DFM $X10^{14}$	R_{NOR} $X10^{11}$	BV_{NOR}	#s.c.	DFM $X10^{12}$	#s.c. 1-I.F	#s.c. 2-I.F	R_{IF} $X10^{22}$	CDFM $X10^{53}$	CDFM $X10^{53}$
1-7	290	163	3	463	6.3	480	5	292	1	0	72.4	98	
9-2	51.6	545	0	281	22.6	523	0	1185	0	8	1624	5406	
9-8	12.7	254	0	32	5.6	243	0	135	2	3	133	5.8	
2-22	316	530	2	1651	8.26	560	0	463	1	1	131	998	
2-8	1183	580	4	6685	10.1	520	4	512	2	1	189	6463	
2-15	394	467	1	1829	14.3	467	0	666	3	6	561	6832	
2-2	728	446	0	3248	11.5	442	0	508	0	4	415	6852	
7-2	17.3	394	1	678	4.5	383	2	171	0	2	117	125	
7-13	98.6	413	2	402	5.4	431	2	229	0	1	167	154	
3-23	1495	568	2	8380	9.96	568	34	439	0	0	157	5776	
3-9	759	491	23	3165	4.3	418	31	143	0	1	42	190	
3-6	1291	482	1	6178	4.9	450	1	218	2	1	58	780	
7-25	99	545	2	534	13.3	482	1	637	0	1	455	1548	
7-15	0.07	413	0	0.31	0.18	500	2	8.8	1	2	4.4	~0	
7-14	40.3	365	2	145	7.36	459	0	338	1	5	87	43	
3-25	197	444	27	720	26.5	600	55	1014	1	1	527	3849	
5-14	s.c.	s.c.	76	-	s.c.	-	76	-	0	1	0.02	-	
5-21	0.6	220	2	1.3	0.98	355	2	34.3	0	1	1.2	~0	
8-3	0.01	257	3	0.03	0.98	193	2	18.7	0	2	2.0	~0	
5-3	11.6	450	11	48.6	0.84	365	20	26.6	0	1	32	0.4	
5-12	430	477	0	2053	8.5	364	0	309	0	1	198	1258	
8-10	338	571	0	193	8.46	386	1	324	0	1	67	42	
9-16	710	310	0	2201	4.98	350	0	174	0	1	51	196	3130
9-25	0.17	250	1	0.43	3.94	238	0	94	0	1	21	~0	0.1
8-18	631	377	0	2379	5.06	343	1	172	1	1	113	463	7400
8-20	129	291	0	376	4.45	282	0	126	1	2	52	25	397
8-22	118	392	0	464	4.3	390	0	168	0	1	56	44	697
8-24	271	377	1	1013	5.7	360	1	203	1	2	143	294	4679
8-25	126	320	0	404	4.45	184	0	82	0	2	65	22	349
8-13	835	282	0	2356	8.8	330	1	291	0	3	398	2723	44238

Table 41. Calculated values of dielectric figure of merit (D.F.M.) and the comprehensive D.F.M. for all wafers after final anneal (400°C for 30 minutes for polyimides, and 500°C for 30 minutes for all others).

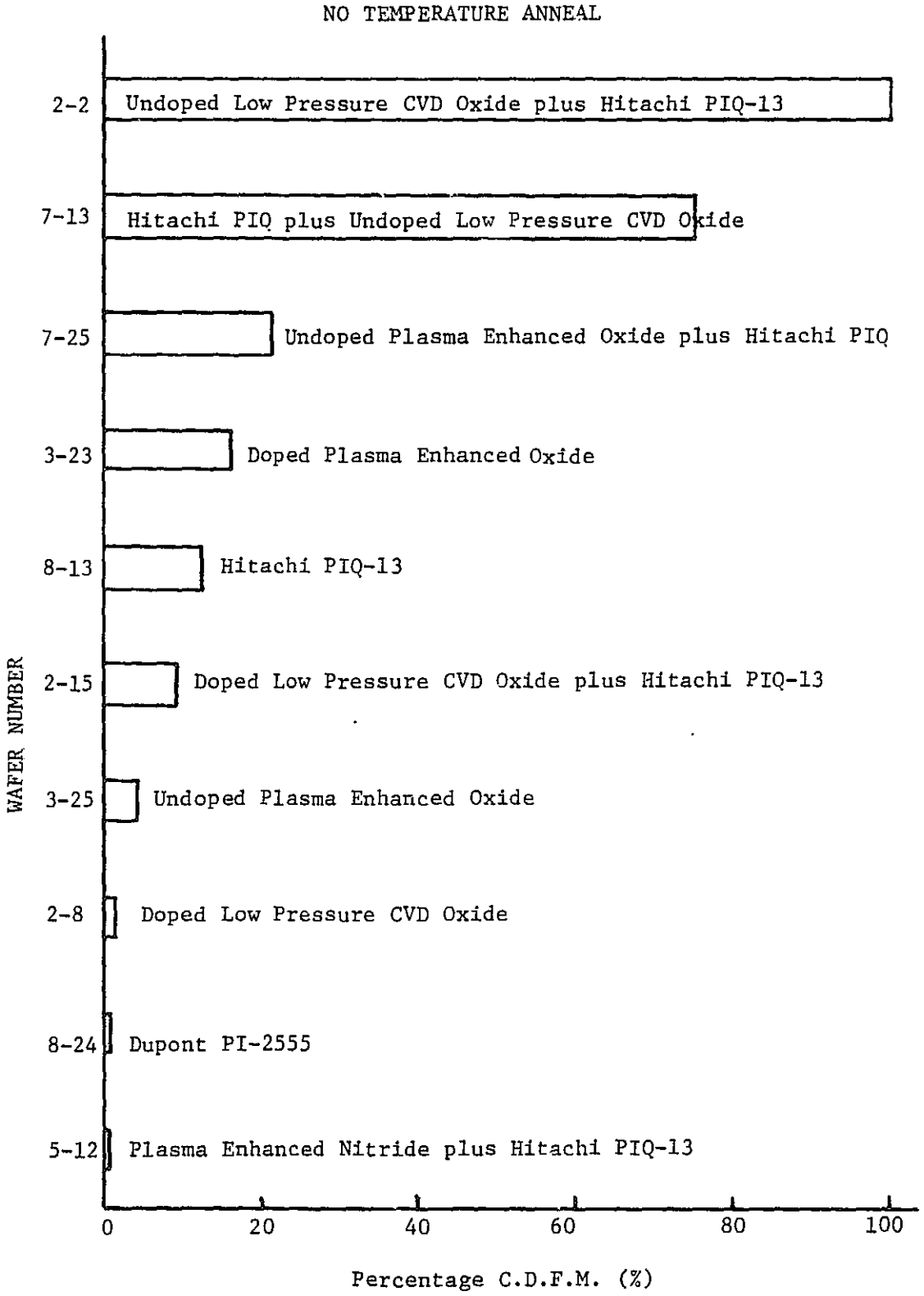


Figure 101. Ranking of the top ten wafers (of the 30 tested) in percentage having the highest C.D.F.M. before any annealing temperatures based on wafer 2-2 (highest) with a C.D.F.M. = $14,367 \times 10^{55}$ volts^2.ohm^4/μm^4.

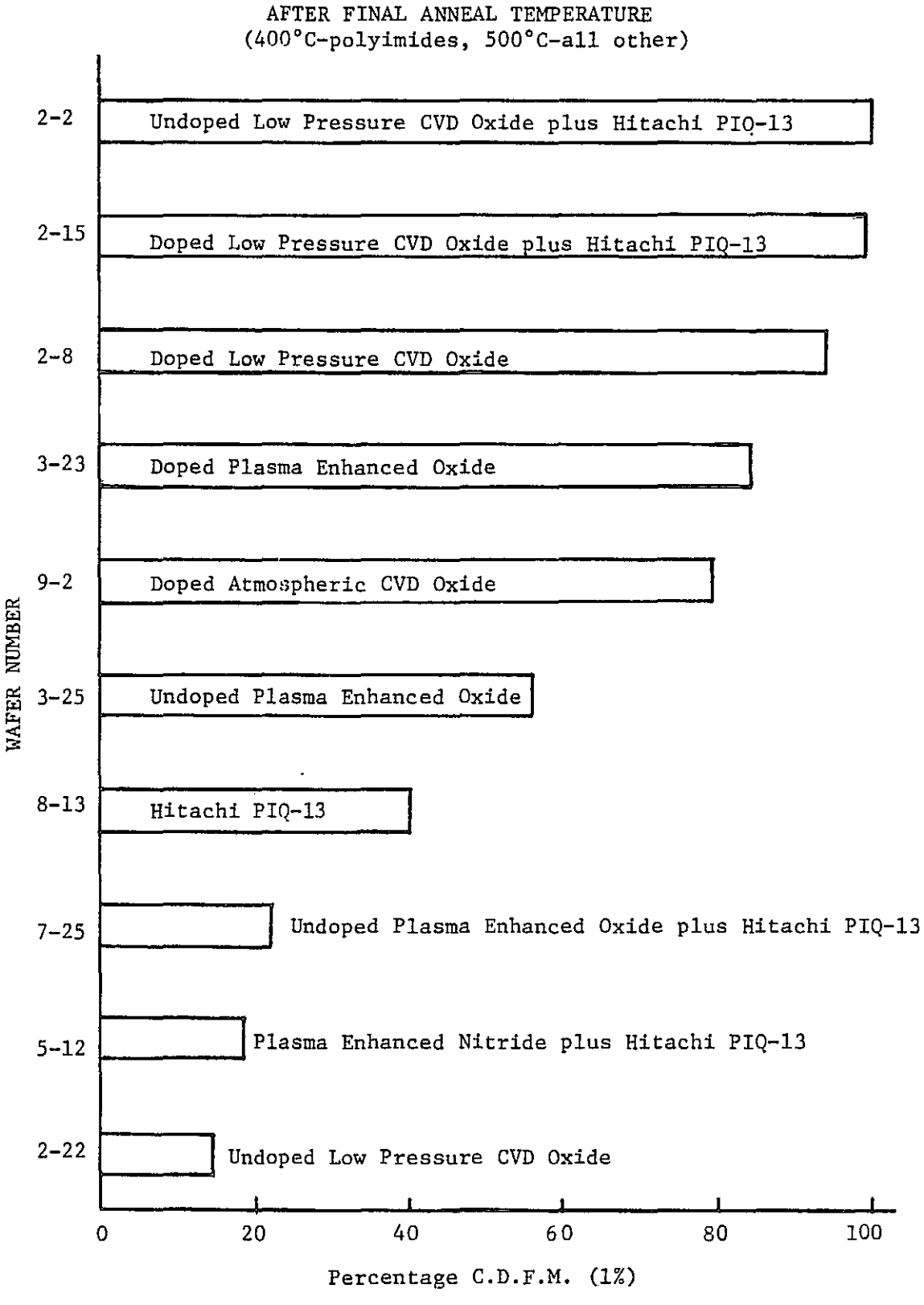


Figure 102. Ranking of the top ten wafers (of the 30 tested) in percentage having the highest C.D.F.M. after final temperature anneal based on wafer 2-2 (highest) with a C.D.F.M. = 6852×10^{53} volts^2.ohm^4/μm^4.

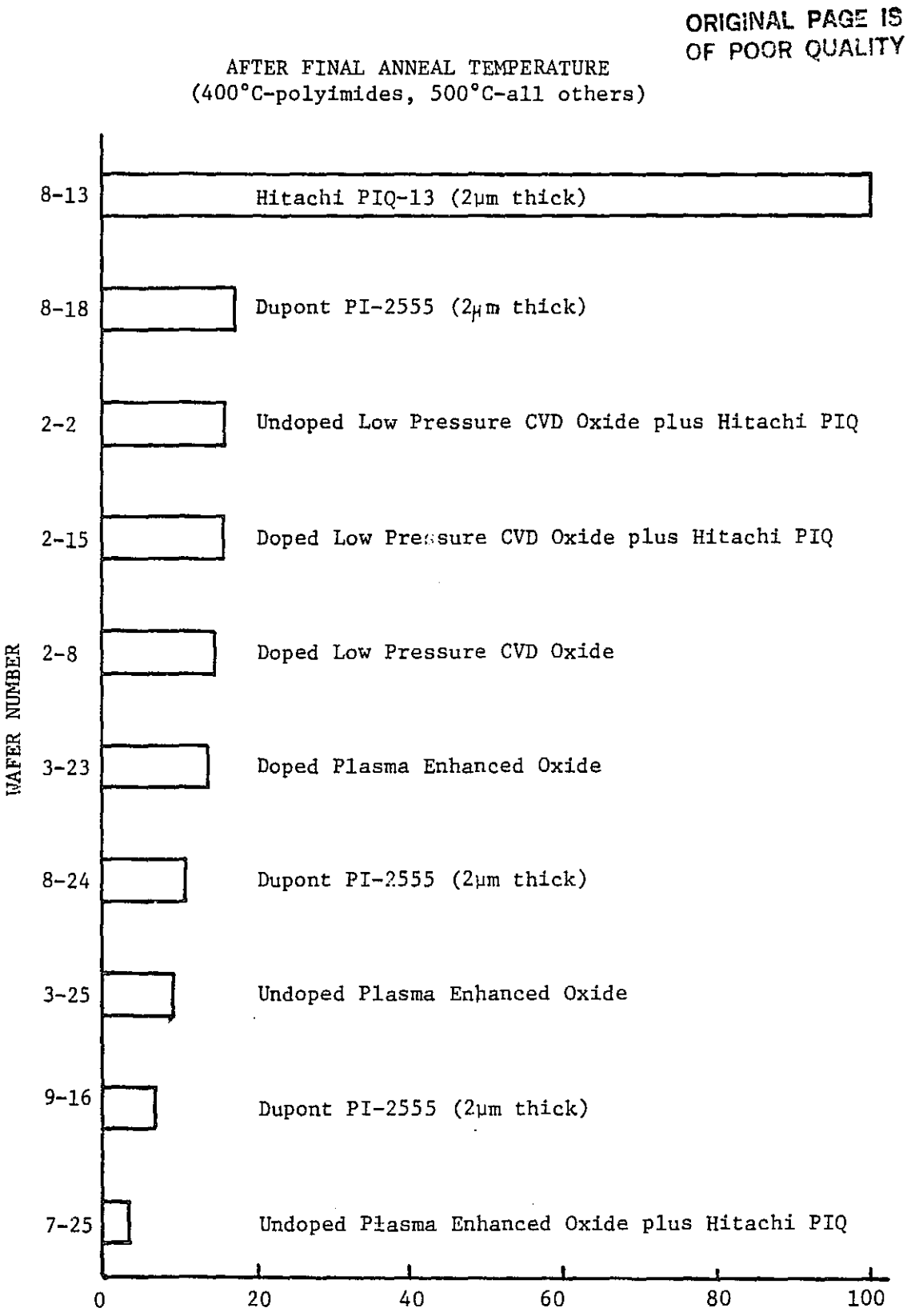
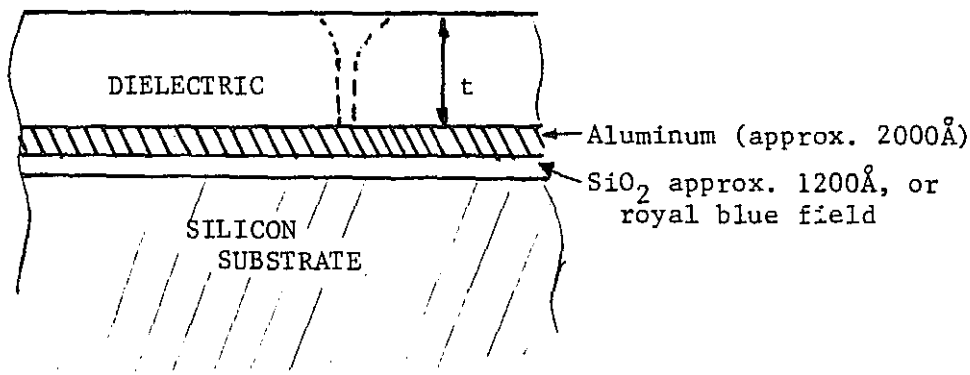


Figure 103. Ranking of the top ten wafers (of the 30 tested) in percentage having the highest C.D.F.M. after final temperature anneal based on wafer 8-13 (highest) assuming two micron thick polyimides whereas all other dielectrics and composits are one micron thick.

D. Pinhole Count

Using the decoration technique, the procedure is as follows:



1. Deposit dielectric (or combination of dielectrics) as indicated above.

2. Dip wafer in hot phosphoric acid a time equivalent to 3 to 5 times the aluminum thickness etch time. Rinse wafer in D.I. H_2O.

3. Strip dielectric.

4. Monitor etch pits in Al (dark blue silicon dioxide field easily distinguished at etched locations). Estimate average pinhole density per unit centimeter.

5. Pinhole density is a function of dielectric material and its thickness.

6. An extenaion of this test can be used to monitor the integrity (ie, pinhole density) of the photoresist used in patterning the dielectric.

Improved results can be obtained if etching in the hot phosphoric acid mixture is accomplished ultrasonically. Typical pinholes as observed in the microscope are shown in Figures 104 and 105.

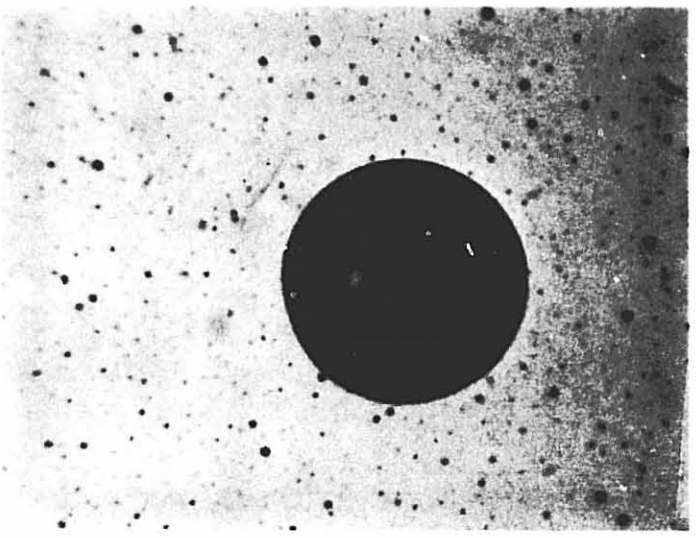


Figure 104. Wafer 4-7. Micrograph of a pin-hole location as etched through low-pressure CVD oxide into the thin aluminum of the test pattern. The oxide has not yet been removed.

Figure 105. Wafer 4-10. A pin-hole in plasma deposited oxide (from Pacific Western) resulting from removing particulates in the scrubber. Notice void where particulate was before scrubber removal.

E. Adhesion and Life Testing

In order to monitor the adhesion of the second level metal to the various dielectrics as well as the adhesion of the dielectrics to the substrate, a pressure-temperature-humidity-bias (PTHB) test chamber had to be constructed. A modified pressure cooker was used as shown in Figure 106, consisting of a heater controlled wafer chuck (temperature monitored with a thermocouple), a couple of wafer probes, a means of introducing an inert gas and a pressure gauge to monitor the pressure accurately. The complete set-up is shown in Figure 107.

A summary of the number of pinholes as determined from the decoration test and the adhesion characteristics of top metal to the dielectric and also the dielectric to the substrate (over aluminum) using the scotch tape stress tape is given in Table 42. The presence of pinholes in the dielectric was first determined by measuring the resistance between the top and bottom level metals (of lot MS4) for the whole wafer covered with metal. All were short circuited. Next, the top level metal was patterned into one centimeter squares, with each wafer having 14 to 16 whole one square centimeter areas. The number of these squares which were open circuited compared to the total is given in Table 42 as the first column under the pinhole test data. These wafers were next exposed to room temperature water, boiling water and pressurized steam (15 psi) for 15 minutes each. After each exposure to water, the wafers were spun dry and dehydrated at $80^{o}C$ in an oven for 15 minutes. Using Scotch tape securely attached

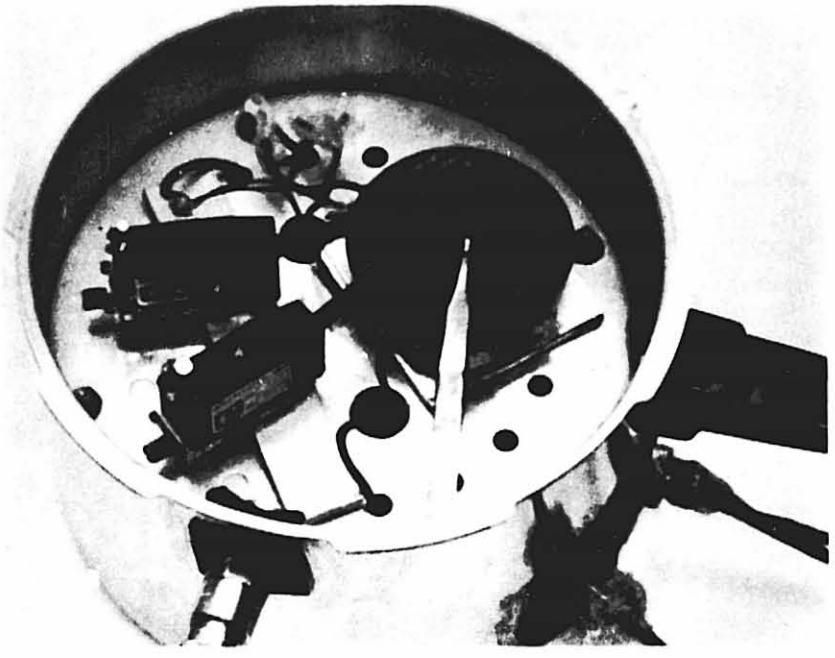


Figure 106. Illustration of pressure cooker arranged for making pressure-temperature-humidity-bias test.

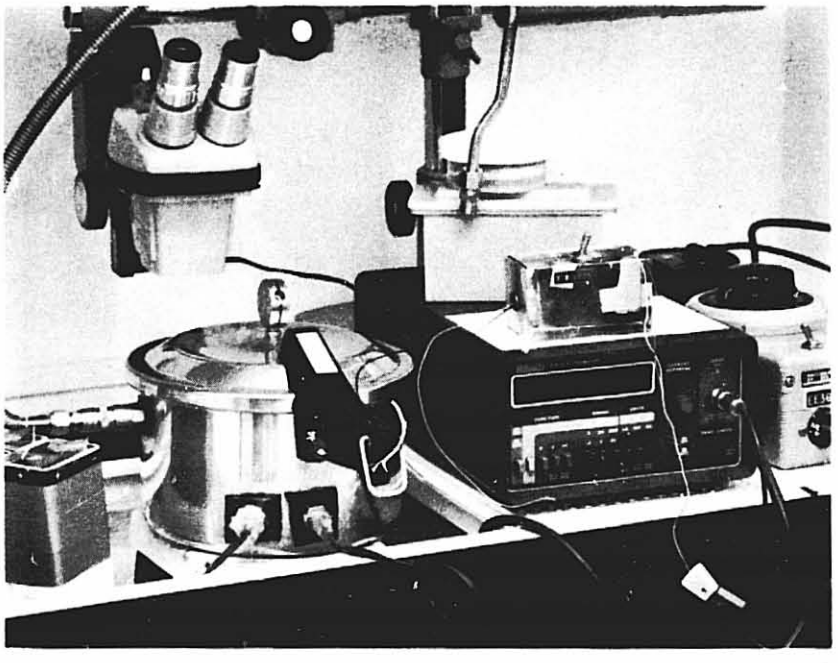


Figure 107. Complete set-up for making pressure-temperature-humidity-bias (PTHB) test on dielectrics.

to the surface, a rapid pull of the tape perpendicular to the wafer removes a portion of the top level metal in some cases. The percentage of top metal removed is given in Table 42. It should be noted that prior to performing the top metal adhesion test, it was attempted to pattern the dielectric using the top 1 cm^2 metal squares as a mask. The oxides were rather easily patterned, but the polyimides had to be left in hydrazine for an extended period of time (2 hours). This dielectric patterning attempt probably affected the top metal adhesion tests.

Next, the top level metal was removed in a hot phosphoric mixture and then allowed to sit in the ultrasonic etch for a period of time (15 minutes). This allowed the etching of the bottom metal through the dielectric pinholes. The average number of pinholes counted per dielectric is given in Table 42.

After counting the pinholes using a calibrated microscope, the wafers were exposed to room temperature water, boiling water and pressurized steam again such that the Scotch tape adhesion test could be performed on the dielectrics. The percentage dielectric lifted is given in Table 42.

PINHOLE TEST WAFERS	DIELECTRIC TYPE	PINHOLE TEST			SCOTCH TAPE TEST (% lift-off)					
					Top Metal			Dielectric		
		$\frac{1cm^2}{(o.c./tot)}$	$\frac{1cm^2}{\%o.c.}$	Avg. # pinholes per cm^2	25°C H_2O 15 min	100°C H_2O 15 min	15psi 120°C 15min.	25°C H_2O 15min	100°C H_2O 30min.	15psi 120°C 30min.
4-6	1μD-LP-Ox	0/14	0	6.3(j)	0(a)	0(a)	0(a)	90	95	95
4-7	1μD-LP-Ox	0/14	0	8.3	0(a)	0(a)	0(a)	60	70	70
4-8	0.25μ D-LP-Ox+PIQ	16/16	100	1.2	90(b)	95	100(c)	100	100	100
4-9	1μD-PE-Ox	15/15	100	0.2	0(a)	0(a)	0(a)	90	95	95
4-10	1μD-PE-Ox	13/13	100	0.3	0(a)	0(a)	0(a)	95	95	95
4-11	0.25μD-PE-Ox+PIQ	13/14	93	0.25	0	0	0	100	100	100
4-12	1μPE-Nit	11/14	79	1.1	0	0	0	15	15	15
4-13	0.25μPE-Nit + PIQ	16/16	100	0.2	0	0	0	95	100	100
4-14	0.5μ Qtz	0/13	0	>100	0(d)	0(d)	0(d)	90	80(k)	95
4-15	0.1μQtz+PIQ	13/14	93	1.0	0	0	0	65	65	65
4-16	PIQ+0.25μD-LP-Ox	8/14	57	0.4	0(e)	0(e)	0(e)	65	70	76
4-17	PIQ+0.25μD-PE-Ox	-	-	2.0	100	100	100(f)	100	100	100
4-18	PIQ+0.25μPE-Nit	14/14	100	0.08	0(g)	0(g)	0(g)	0	0	5
4-19	PIQ+0.1μQtz	-	-	10	(h)	(h)	(h)	100	100	100
4-20	0.4μD-Ox+PIQ	14/14	100	0.7	80(i)	90	100	90	100	100
4-21	0.7μPIQ	6/14	43	>100	90(i)	95	100	95	100	95
4-22	0.75μPI-2555	0/14	0	13.1	90(i)	95	100	95	95	100
4-23	1.2μ PIQ	8/16	50	1.3	50(i)	70	100	95	95	100
4-24	1.2μ PI-2555	5/14	36	18.7	85(i)	95	100	95	100	100

NOTES:

s.c. = short circuit
o.c. = open circuit (resistance measurement between metals utilized mercury probe)
(a) top metal did not lift but oxide in the scribe lines did lift off
(b) 90% top metal lifted plus 20% of the polyimide lifted
(c) 100% top metal lifted plus 90% of the polyimide lifted
(d) quartz in scribe lines lifted
(e) oxide in scribe lines lifted, polyimide stayed
(f) all metal lifted, break at oxide-polyimide interface
(g) nitride in scribe lines lifted
(h) top metal was removed in prior processing
(i) wafer had been in hydrazine for 2 hours trying to pattern polyimide in scribe lines prior to this test
(j) average number of squares inspected was 8, inspection made by microscope
(k) one area on wafer exhibited excellent adherence

Table 42. A summary of the number of pinholes as determined from the decoration test and the adhesion characteristic of top metal to the dielectric and also the dielectric to the substrate (over aluminum) using the Scotch tape stress test.

V. CONCLUSIONS AND RECOMMENDATIONS

Based upon the defined comprehensive dielectric figure of merit (C.D.F.M.) after final anneal temperatures, the low pressure CVD oxide combined with polyimide as well as low pressure CVD oxides and plasma enhanced oxides by themselves look very promising. Similar results are observed for these dielectrics having no temperature anneal. If two micron thick polyimides are allowed to be compared to all other dielectrics which are one micron thick (since they do not increase in stress with increased thickness and since most polyimides used in the semiconductor industry today are 1.5 to 2 microns in thickness), then polyimides look very promising.

It should be noted that the thickness of the dielectrics on wafer lot MS4 (the pinhole test wafers) was not measured, and from the pinhole count results, it is suspected that much thinner dielectrics existed on these wafers (especially for polyimides) than anticipated, or the fact that too many experiments were conducted on these wafers to render representative results may be an equally valid explanation.

It should also be noted that the sputtered quartz as received from the vendor was thin and enhibited poor adherence to the substrate. Much of this dielectric was removed in attempting to pattern via holes in the thin quartz (1000 Å) for use with polyimide composites prior to depositing second level metal. Thus, it exhibited the poorest qualifications as a dielectric as determined from our testing procedure.

For future recommendations, it is suggested that an investigation of other dielectric combinations be conducted. In the study just completed, only dielectrics by themselves (atmospheric, LPCVD, plasma and sputtered oxides, plasma nitrides and polyimide) or these dielectrics combined with polyimide were investigated. To complete this study, a look at other dielectric combinations should be undertaken and their advantages utilized (i.e., by depositing a more denser plasma oxide first and then followed by a less denser low pressure or atmospheric oxide, excellent via wall slopes may be realized in patterning this combination; nitride over polyimide proved excellent in the present study in pinhole density and film adhesion under pressurized steam, what about nitride over oxides, etc.)